IBM Field Engineering

Maintenance Manual

System/360 Model 40

2040 Processing Unit

SY22-2841-3

Preface

This manual contains information for servicing the IBM 2040 Processing Unit.

The section on Diagnostic Techniques gives general information concerning the maintenance concepts for System/360, and also procedures and guides for trouble-shooting. A useful description of the Diagnose instruction is given in this section. The Maintenance Features section contains a description of console displays, information on use of the console, detailed explanation for internal diagnostics, and log-out charts (with an example of a SEREP print-out). Preventive Maintenance describes and tabulates preventive maintenance action and frequency. There is a section on Checks, Adjustments, and Removals (which includes both the High Frequency and Mid-Pac power supplies). The section on Locations uses charts, diagrams, and pictures to give quick, visual reference to CPU locations.

We recommend placing this manual in a binder with the staples removed. The first page of major sections, and charts or examples could be tabbed for quick reference.

Information in this manual supplements that in the following publications:

System/360 Model 40, 2040 Processing Unit Diagrams Manual, Order No. SY22-2842

System/360 Model 40 Comprehensive Introduction, FETOM, Order No. SY22-2840

System/360 Model 40 Functional Units, FEMI, Order No. SY22-2843

System/360 Model 40 Theory of Operation, FEMI, Order No. SY22-2844

System/360 Model 40 Power Supplies and Appendices, FEMI, Order No. S223-2845

SLT manuals:

Solid Logic Technology, Packaging, Tools, and Wiring Change, FETOM, Order No. SY22-2800

Solid Logic Technology, Power Supplies, FETOM, Order No. SY22-2799

This manual is written to engineering change level 254814 for ALD's and CLD level 255263. Subsequent engineering changes may alter the contents of this manual.

All three-digit figure references are to *System/360 Model 40, 2040 Processing Unit, Field Engineering Diagrams Manual,* Order No. SY22-2842.

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Changes are periodically made to the specifications herein; any such change will be reported in subsequent revisions or Technical Newsletters.

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Safety cannot be overemphasized. To insure your personal safety and the safety of co-workers, make it an everyday practice to observe safety precautions at all times. You should be familiar with the general safety practices and procedures for performing artificial respiration outlined in IBM Form 124-0002.

Always use a reliable voltmeter to verify that power is actually off after using power-off switches.

Although all power supplies are provided with bleeder resistors to drain off capacitor charges when power is dropped, it is wise to check all capacitors with a meter before attempting maintenance. A defective bleeder resistor could create an unexpected hazard.

NOTE: In a multi-system complex, if the EPO bypass switch must be activated to isolate a system, deactivate the switch as soon as possible. The proper procedure is outlined in "Dual/Multi-System Emergency Power Off (EPO)."

Abbreviations

A0	A Register byte 0
A1	A Register byte 1
AX	A Register Extension
ALU	Arithmetic and Logic Unit
AMWP	Bits 12-15 of the PSW
A Reg	A Register
ASCII	American Standard Code for Information Interchange
B	Base Register
BCD	Binary Coded Decimal
BCDIC	Binary Coded Decimal Interchange Code
B Reg	B Register
CAS	Control Automation System
CAW	Channel Address Word
CC	Chain Command
CC	Condition Code
CCW	Channel Command Word
CDA	Chain Data Address
CE	Channel End
CI	Command Immediate
CLD	CAS Logic Diagram
CLFC	Condensed Logic Flow Chart
COBOL	Common Business Oriented Language
CPU	Central Processing Unit
C Reg	C Register
CSW	Channel Status Word
CT	Count
CU	Control Unit
CX	C Register Extension
C0	C Register byte 0
C1	C Register byte 1
D	Displacement Address
D Reg	D Register
D0	D Register byte 0
D1	D Register byte 1
DE	Device End
Decr	Decrement
Del	Delayed
Des	Destination
DM	Diagnostic Monitor
EBCDIC	Extended Binary Coded Decimal Interchange Code
EC	Engineering Change
ECAD	Error Checking Analysis Diagram
EREP	Environment Record Edit and Print
FNB	Functional Branch
FORTRAN	Formula Translating System
FP	Floating Point
GP	General Purpose (Registers)
HEX	Hexadecimal
HIO	Halt I/O (Input/Output)
I	Immediate Data (not in text)
IB	Instruction Buffer
IC	Instruction Count
ICC	Interface Control Check
ID	Inhibit Dump
IDQ	Invalid Decimal Digit (on Q bus)
IF	Interface
ILC	Instruction Length Code
I/O	Input/Output
IOCS	Input/Output Control System
IPL	Initial Program Load
IR	Interrupt Request
ISA	Invalid Storage Address
ISK	Insert Storage Key
IZT	Integrated Zero Test
L	Operand Length
LDB	Load Button
LS	Local Storage
LSAR	Local Storage Address Register
LSD	Least Significant Digit
MAP	Maintenance Analysis Procedure
MC	Machine Check
MDM	Maintenance Diagram Manual
MI	Maskable Interrupt
MS	Main Storage
MSC	Machine Status Chart
MSD	Most Significant Digit
MSS	Manual Single Shot
OS	Operating System
P	Parity (bit)
PC	Parity Check
PCI	Program Control Interrupt
PG	Parity Generation
PRI	Program Interrupt
Prg Chk	Program Check
PSA	Protected Storage Address
PSW	Program Status Word
Pty	Parity
Rx	Operand Register
ROAR	Read Only Address Register
ROBAR	Read Only Back-up Address Register
ROS	Read Only Storage
ROSCAR	ROS Channel Address Register
RR	Register-to-register operations
R Reg	R Register
RS	Register-to-storage operations
rtpt	reinterpret
RX	Register-to-indexed-storage operations
RX	R Register Extensions
R0	R Register byte 0
R1	R Register byte 1
R/W	Read/write
SAB	Storage Address Bus
SAT	Storage Address Test
SC	Selector Channel
SER	System Environment Recording
SEREP	System Environment Record Edit and Print
SI	Storage-and-immediate-operand operation
SIO	Start I/O (Input/Output)
SILI	Suppress Incorrect Length Indicator
SLT	Solid Logic Technology
SMS	Standard Modular System
SP	Storage Protect
SPLS	Storage Protect Local Storage
S Reg	S Register
SS	Storage-to-storage operation
SSK	Set Storage Key
STATS	Staticizer Latches
SVC	Supervisor call (op code)
SX	S Register Extension
S0	S Register byte 0
S1	S Register byte 1
TCH	Test Channel
TIC	Transfer in Channel
TIO	Test I/O (Input/Output)
TROS	Transformer Read Only Storage
UBA	Use Bump Address
UCW	Unit Control Word
Unobt	Unobtainable
WLR	Wrong Length Record
X	Index Register
YC	Carry Latch
YCH 1, 3	Selector Channel Stats 1, 3
YCI	Indirect Function Carry Stat
YCD	Direct Function Carry Stat
μP	Microprogram

Maintenance Concepts

The IBM System/360 Model 40 provides features to assist the customer engineer in: failure location, fault location, deferred maintenance and rapid repair.

Fault Location

After a system malfunction has been detected, the troubleshooting aids available to the customer engineer are: indicators and manual controls, internal diagnostics, external diagnostics, external maintenance programs and supporting documentation.

Deferred Maintenance

The log out facility allows deferred maintenance. Certain failures are such that long periods of time elapse between interruptions. Troubleshooting this type of fault is time-consuming. The failure is difficult to reproduce.

The customer often prefers to continue system operation and postpone maintenance activity. The log out feature, by providing the customer engineer with system information at the time of the error, allows deferred maintenance.

When the system detects an error, the current micro-routine is stopped and the machine branches to the log out routine. A number of logic-controlled cycles followed by a micro-routine transfers machine data into main storage. Programs are available to produce a printed copy of this information.

The log out data contains the information obtainable by analyzing a hardstop condition from the console. A full description of the log out feature is given in "Log Out."

Maintenance Compatibility Among System/360 Models

Basic maintenance philosophy is the same for all models. Where possible, the maintenance features are identical. Obviously, all logic circuit-dependent features have to be related to the specific model.

Principal non-compatible features are fault-locating facilities and the log out format.

Principal compatible features are: maintenance of components (SLT, ROS, Storages), maintenance of I/O equipment, format of documents, diagnostic monitors, reliability test programs, and I/O diagnostics.

Fault Location Philosophy

The system normally cannot tell which component is failing. Error detection and maintenance features built into the system, with back-up documentation and external diagnostics, give powerful assistance if properly interpreted.

The normal trouble-shooting procedure is:

1. CE call
2. Collect error information
3. Interpret error
4. Determine machine unit that failed
5. Reproduce error; find smallest possible error environment
6. Localize failure
7. Repair and check
8. Reports

Documentation

Diagrams Manual (DM)

The following paragraphs explain the philosophy behind the compilation of the DM and instructions for its use.

System Data Flow Diagram

This shows over-all data flow of the 2040 and shows exits and entries to channels.

Unit Data and Control Diagram (UDCD)

This expands each unit contained within the system data flow diagram to include major controls.

I/O Operations Diagram

This is a positive logic diagram showing the over-all function of I/O operations.

Simplified Logic Diagrams (SLD)

These are logic diagrams of those complex areas of the system where the ALD's might confuse.

Condensed Logic Flow Chart (CLFC)

These show in condensed form the concept of a particular routine to facilitate reading of CAS Logic Diagrams (CLD's).

Malfunction Analysis Procedure Diagram (MAP's)

MAP's are designed to supplement customer engineering training and experience.

They provide a planned approach to malfunction environment in the field.

Over-all System MAP's

The over-all system MAP provides the initial key to the general fault-analysis problem. The problem is one of determining the failing unit (CPU, channel, or I/O) and subsequently the failing sub-unit (main storage, local storage, read only storage, ALU, multiplex or selector channel).

Detailed MAP's

The system unit MAP's supplement the over-all system MAP's and are produced for these areas:

1. Early checks
2. Control checks
3. Late checks
4. Main storage
5. Local storage
6. Read only storage
7. ALU
8. Channels
9. Power

These diagrams direct the customer engineer to a particular ALD sheet or ECAD and describe the procedures in detail.

Other Support Documentation

Machine Status Charts (MSC)

Certain microprograms are supported by machine status charts (MSC's). These charts record the valid machine status of various latches and registers at the end of each specified microinstruction in single-cycle mode. MSC's are provided for: hardware system reset, CPU check-out microprogram, dump/undump, selector channel checkout and initial program load microprogram (IPL).

Hardware system reset must be executed successfully before entering CPU checkout. Thus, hardware system-reset status provides a basic checking point in machine operation.

This can be displayed on the console panel by depressing the system-reset pushbutton in single-cycle mode and the operation checked with the hardware system-reset machine status chart. System-reset is immediately followed by the CPU check-out microprogram. (Press system reset in process mode.)

Machine status charts also contain, where applicable, diagnostic hints in the form of descriptive notes.

Address Lists

The address lists are contained in the CLD's and provide cross-reference lists for all ROS locations indicating:

1. ROS address
2. Control field punching
3. CLD location
4. EC number
5. Version

Automated Logic Diagrams (ALD's)

ALD's are computer-generated schematics representing machine functions. Circuits are shown as blocks which symbolize logical functions. They are connected by printed lines to show electrical connections; inputs enter the circuit on the left, outputs leave at the right.

CAS Logic Diagrams (CLD's)

CLD's are printed drawings representing the various micro-routines. The micro-instructions are shown as blocks connected to each other to indicate actual micro-instruction sequence.

Error Check Analysis Diagram (ECAD's)

- **ECAD's assist in error analysis by indicating the logic that produces the error condition.**
- **ECAD's allow the user to start from the error indicator and work backwards.**

These diagrams show simplified logic of each checking circuit and the logic of all incoming paths as far back as the previous check. The information provided by the CPU check-out machine status charts should, in case of logic-detected errors, be sufficient to identify the failing path.

These diagrams are effective fault-locating documents, as they show the way from console indicators (or log out information) directly to the circuitry affected.

NOTE: These simplified logic diagrams are actual machine circuits; they are therefore EC-level sensitive.

Timing Chart (TC)

Timing charts are diagrams depicting the timing conditions of applicable operations.

ROS Control Field Chart

These are charts for every ROS control field which indicate bit configuration; ROS mnemonic used on CLD's; and function performed by the field.

External Diagnostics

External diagnostics (machine language programs stored on cards, tape, etc.) are provided to check and verify system operation from the operating level covered by internal (microprogram) diagnostics, to the level where the system can safely be handed over to the customer.

These programs should be used in:

Initial installation check-out
Unscheduled maintenance (trouble-shooting)
Scheduled maintenance

EC and RPQ verification
Check-out of specific system components (I/O units) during customer operation.

Like all programs for System/360, the maintenance programs are designed to run under control of a monitor program. The diagnostic monitor (DM) takes care of all common housekeeping operations, handles interrupts, and provides the interface between the customer engineer and the system.

The actual maintenance programs (diagnostic sections) contain only program segments (diagnostic routines) which deal with actual tests and diagnostics and can run only under DM control.

If the system is unable to run a diagnostic monitor, special bring up programs are provided to build it up from the point of successful running of internal diagnostics to the level where a DM can operate properly.

The various levels of external diagnostics and the system debug order are:

Bring up monitors
Diagnostic sections which can be run under the bring up monitor
DMA8 (Diagnostic Monitor A8)
Remainder of CPU sections under DMA8
Channel and I/O sections under DMA8
MIDAS system test, if available.

Diagnostic Monitors (DM's)

The diagnostic monitor program has these functions:

1. Searching for the required diagnostic program (from tape, disk, etc.).
2. Allocation of storage and I/O units for its use.
3. Loading and relocation.
4. Translation of output messages generated by the diagnostic program into a form suitable for the output device in use.
5. Translation of a standard set of input messages into a form appropriate to the program in use.
6. Provision of input subroutines, such as entering certain information patterns into storage.
7. Buffering of output messages for most efficient use of the system.
8. Providing for overlapping the execution of one diagnostic program with the loading of the subsequent ones.
9. Handling all interruptions while diagnostic programs are being run.
10. Protection of each program from interference by other diagnostic programs and external influences.
11. Provision of sub-routines common to several programs.

The use of diagnostic monitor programs has these advantages:

1. The diagnostic programs may be written by independent design groups.
2. One diagnostic program may be used with any monitor program in an appropriate system.
3. The customer engineer does not have to use different loading techniques for the different programs.
4. It allows fault-finding to take place under conditions similar to those encountered while customers' programs are being run.
5. There are several diagnostic monitor programs to satisfy the variable conditions that can occur throughout the System/360.

The basic difference between DM's is their amount of operating features (or, the number of main-storage locations they may occupy). DM's are program compatible among the various System/360 models, provided that the configurations specified are met. (Main parameter is the core storage size.)

The standard monitor for a smaller model may be used as a bring up monitor for a large system.

On the IBM 2040 the following monitors are used:

1. Bring up monitor for 2040 (DM1)
2. DMA8 — Standard Programs
3. DMK — Emulator Programs

DM1: The bring up DM uses the half-word instructions debugged by the bring up programs. This monitor can be used to debug the instructions necessary to provide the DMA instruction set (small binary).

DMA8: DMA8 is designed for small systems having a minimum of 16K main storage. DMA8 requires 8K on a 16K machine and 12K on 32K, and higher, machines.

Any standard diagnostic section runs under DMA. All types of interrupts can be handled; interrupts expected by the sections are returned to it, unexpected interrupts cause error messages. Loading and printing are not overlapped with execution of the section.

DMA8 uses a full complement of input messages that are entered through the 1052. A limited number of messages may be entered through the console if a 1052 is not present.

DMA8 is a stand-alone monitor and can only be loaded by IPL.

Diagnostic Sections

Four types of programs are available.

Functional Tests (Reliability Tests)

These tests are used to verify the overall reliability of the system. They are used to discover whether a general system area is fault free.

The design of these tests provides thorough detection coverage, short running time and minimal size. These programs do not locate faults at circuit level. However, a sufficient variety of numerical examples is provided to permit manual check-out of the failing instruction.

Circuit Level Tests

These programs are used as fault-locating tools for particular system components. They make available extensive information about any failures that these programs discover. This information, when analyzed, is sufficient to determine a relatively small area of circuitry.

Tests in this group make extensive use of the diagnose instruction, and are valid only on the model for which they are designed.

Measurement Tests

This is a group of I/O programs designed to measure a specific parameter, such as the length of inter-record gaps, or to facilitate manual adjustments, such as mechanical clearances and linkages.

Check-Circuit Tests

These tests are designed to use logic and program facilities to give a positive test of checking circuits.

System Failure Detection

- **Error detection by logic circuits.**
- **Error detection by microprogram.**
- **Error detection by internal diagnostics.**
- **Error detection by external diagnostics.**

Error Detection by Logic Circuits

Reference to the System Data Flow Diagram in the *IBM System/360 Model 40, 2040 Processing Unit, Field Engineering Diagrams Manual,* Form 223-2842, shows the comprehensive checking provided in the IBM 2040 for both data and control paths. Each check is individually indicated on the console panel or internal CE panel and, where applicable, an over-all check light is also provided (i.e., two-wire checks).

The CPU is comprehensively checked mainly by parity check circuits. All data transfers between registers and between registers and main storage are checked. Good parity is always written into main storage.

Parity checking is also used on the Read Only Storage (ROS), both at the address and at the output. In addition, the ROS decoder outputs are checked for validity.

The ALU function decoder is parity checked. Inside the ALU, signals are generated independently in true and complement form and checks are made to ensure that these signals are correctly propagated throughout this unit (ALU two-wire checking).

To reduce maintenance time, the individual error checks are OR'ed in groups by timing and function, into three over-all check latches: the control check latch, early check latch and late check latch. These over-all check latches are separately indicated.

The outputs of the three over-all check latches are OR'ed together to produce the signal, Error Will Stop Clock, which stops the T clock on completion of the machine cycle in which the error was detected and raises several inhibit lines.

If the failure results in a control or early check, the ROS inhibit line will be raised early enough in the cycle to prevent any change of the ROS sense latch settings. The purpose of these inhibit lines is prevention of the loss of valuable diagnostic data.

The OR of the three over-all check latches is also used to set the master check latch.

Error Detection by Microprogram

Some machine errors are detected by the microprogram: in the CPU, by invalid branches of the microprogram to unused locations (the TROS tapes at these locations contain the function LOG); in the channels, by time out conditions on the interface signal-sequence. The microprogram sets the interface control check, which, in turn, causes the same sequence as an error detected by logic checks.

In all microprogram routines, various tests for programming errors and exceptional conditions are made. Included are tests for valid op code, valid specification of operands, storage protect violation, invalid addresses, and valid data. Arithmetic operations test for unusual conditions such as overflow and divide exceptions.

Detection of any of these conditions leads to a program check interrupt rather than to a possible machine check, greatly reducing the number of program or machine problems.

Errors detected by microprogram in the CPU raise one of these signals:

Start Log Out
Stop T Clock

Start Log Out

A microprogram-generated control signal, LOG (CB = 2; CD = 3), is provided to give the signal, Start Log Out. LOG is used in all invalid microprogram words to give a log out, showing that an unused word has been addressed or an invalid branch taken.

Invalid branches also contain, as next address, the address of the branch that probably should have been taken. This allows the machine to continue processing the original instruction if it is in error disable mode.

When the signal, Start Log Out, is given in error disable mode, it is latched up as a control check and results in a log out when the machine is enabled.

Stop T Clock

A microprogram-generated control signal, STOP (CB = 5; CD = 3), is provided to give the signal, Stop T Clock. It is used only in diagnostic microprograms and results in a machine hardstop provided that errors are enabled. The signal is also OR'ed into the early check latch to make possible check restart during the CPU checkout diagnostic microprogram.

Error Detection by Internal Diagnostics

Most of the circuits that are not continuously monitored by logic checking are periodically checked by the CPU check-out routine. This routine, of approximately 75 microinstructions, is executed when system power is brought up and every time initial program load or system reset on the console is pressed.

In addition, the check-out is performed during the machine check interrupt sequence and can be looped for trouble-shooting purposes.

Other diagnostic microroutines are built into the system to provide an easy way of checking some circuits. Routines included are:

Main storage worst pattern test
Main storage addressing test
Local storage worst pattern test
Local storage addressing test
Dump test

These tests are not executed automatically but are controlled from the console.

Error Detection by External Diagnostics

These are detected by running maintenance programs. The programs, when run under diagnostic monitors, upon detection of an error, print out expected and actual results. The context of these results is program-dependent (it may represent a PSW, CSW, etc.). This may be determined from the diagnostic section write up or listing.

System Handling of Errors

The sequence of events following the detection of an error is illustrated in Figure 1.

If the machine is in normal processing mode, the detection of an error stops the T clock at the end of the machine cycle in which the error is detected. Hardware and microprogram log out takes place, CPU check-out and system reset is executed, and finally the current PSW is replaced by the machine check program status word (PSW).

The program, normally the operating system supervisor, then determines the next action to be taken. Errors detected during CPU check-out, system reset, store and load PSW, bring the system into hardstop.

Log out and machine check interrupt can be disabled (console switch or PSW Bit 13 = 0). Errors are still detected and latched up until the machine is again enabled.

Error Stat

The error stat is set by circuitry at the beginning of a log out. It is also set by system reset.

When the error stat is set, all dumps are inhibited and any subsequent errors result in a machine hardstop.

Reset is by microprogram.

Error Resetting

The following methods of error resetting are provided:

System Reset can be initiated by a pushbutton from the console panel or forced by hardware. It resets all errors and returns the CPU and channels to their initial state.

Check Reset is controlled by a pushbutton on the console panel. It resets all check latches, but these latches may be set again by the error data on removal of the reset signal.

Reset Errors is a microprogram-generated control signal CR = 6 and Manual Stat (Y10). As it is active only with the T clock running, it is used only in error disable mode. It resets all check latches.

Other reset signals derived from the above are:

1. Error Reset = System Reset Latch or Check Reset or Reset Errors.
2. Reset Check Latches = Error Reset or Log Out Start T.

Other Error Conditions

The error-checking facilities described so far detail the possibilities for detecting system malfunctions before handling the system over to the customer. The ultimate tests are the correct answers of the customer's machine-language programs.

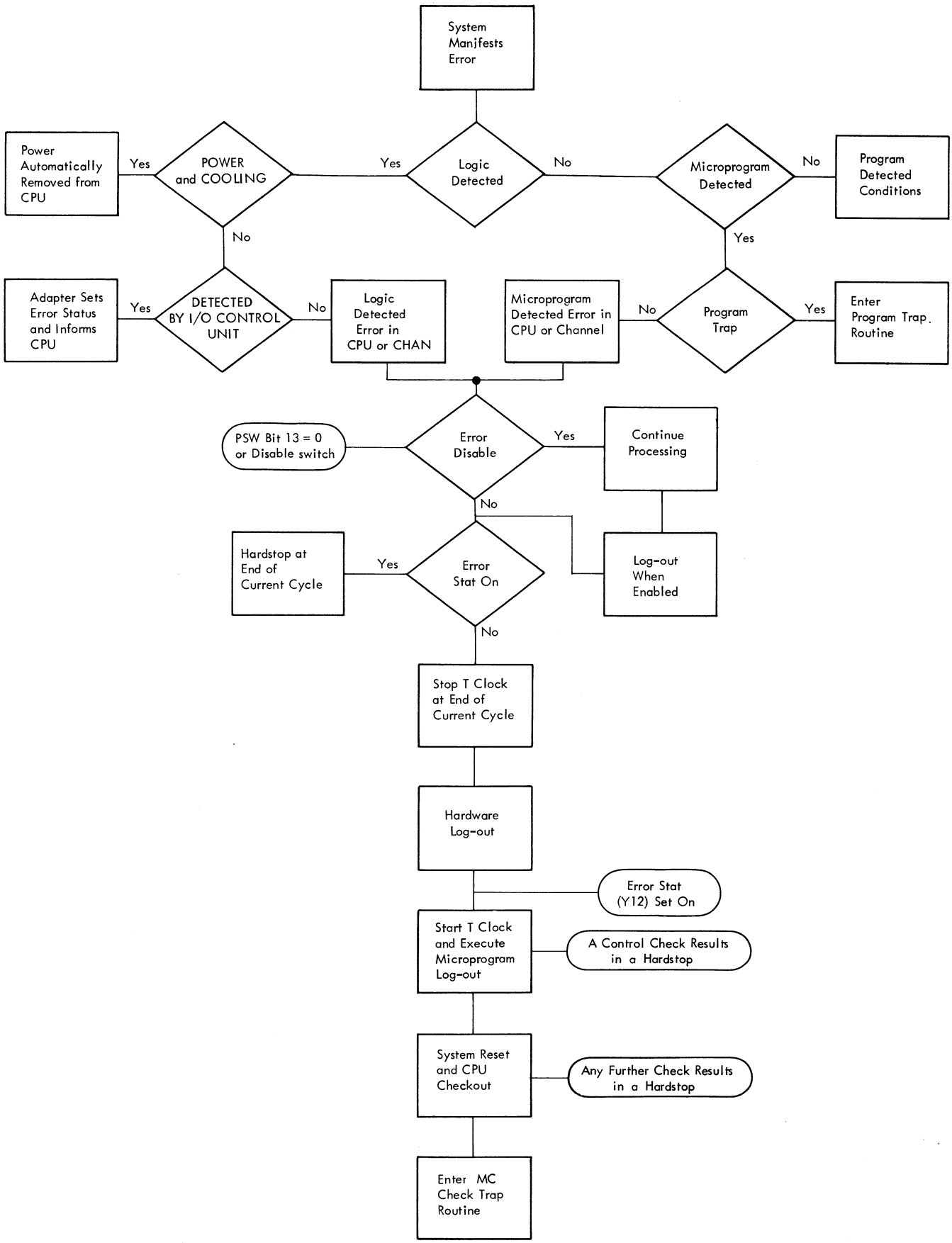


Figure 1. System Handling of Errors

The user's definition of error detection covers only those machine malfunctions which are indicated during execution of his jobs. In the 2040 CPU the checks provided are the hardware checks, micro-program checks and to a certain extent, the CPU check-out routine. These tests cannot give a full coverage of all malfunction possibilities; however, this error detection system is much more powerful in a ROS-controlled machine than in previous machine types, since parity checking not only affects the flow of data through the system but all handling of control information and the control itself.

Customer engineers should be aware of the following machine malfunctions which may occur. (Over-all checking philosophy deals only with single errors):

1. Parity checking discovers only single errors: i.e., dropping or picking of an even number of bits cannot be detected. This may be of special importance for the ROS output where there is one parity bit for 53 data bits.
2. There is limited checking of check circuits.
3. Microprogram B and C branch conditions are checked only by CPU check-out.
4. Invalid microprogram branches are detected only if the branch address is unused and contains the LOG instructions.
5. The CPU check-out tests only basic circuit operations and has no provision for various data and operation patterns.
6. Storage protect compare circuits are not checked.

Diagnose Instruction

The diagnose instruction:

1. Has the RS format.
2. Provides access to any micro-instruction and to certain machine functions for diagnostic purposes.
3. R1 and R3 fields specify the setting of stats YA and YB.
4. B2 and D2 fields specify a ROS address where a diagnose function is to be performed, and the condition of the CPU, ISA, or PSA.
5. Is operative only in supervisor state.

Utilization

The diagnose instruction is a tool for the diagnostic programmer, allowing him to enter the microprogram at any step he desires with the data he chooses. The customer engineer must understand thoroughly the microroutine he intends to enter before attempting to use diagnose. Diagnose is helpful on system faults that do not fail in single cycle mode. If the failure can be narrowed to a few micro-instructions, a scoping loop can be set up. Since the instruction is a programming tool, there is no mnemonic.

The ROS address entry is determined by the setting of the B2-D2 fields of the instruction. The B2 field must be used to accomodate the setting of ISA, PSA or CPU state bits. Setting of the B2-D2 fields require two bytes of data entered from the console switches. Byte 0 contains ISA, PSA, CPU, even parity bit and the high order hex digit of the ROS address.

Byte 1 switches enter the remaining two hex digits of the ROS address. Byte 1 is entered automatically with odd parity; this parity controls the parity of the entire ROS address.

Even parity is forced for the high order hex digit of the ROS address in byte 0. The bit position labeled even parity (Figure 2), is used to control odd parity for the ISA, PSA, or CPU bits; i.e., if these three bits are all off, the even parity bit must be entered.

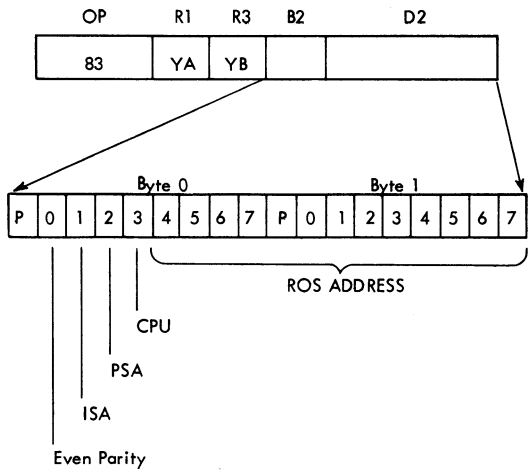


Figure 2. Console Entry for Diagnose Instruction

The stat setting needed when entering a ROS address is forced by making R1-R3 equal to the YA-YB stats. When the diagnose instruction is executed, stats YA-YB are set and the desired ROS address is forced.

Unless the machine is set to stop on ROS in the selected microprogram, it takes an incorrect branch, loops or traps, and the next I fetch is executed. For scoping loops this could be a branch back to the diagnose instruction.

To supply data for the ROS operations, the undump routine in the machine can be used. The dump area of local storage must be set up before the diagnose instruction is executed. An undump can be forced by addressing the ROS address of the undump routine used for multiplex operations. Setting ROAR section of the dump area provides an entry to another ROS address at the completion of undump. Resetting the

dump area after looping (it is empty after use) is also handled by diagnose.

The following program enables an entry at any desired microprogram step by manually setting a main storage area first with the data flow bytes required. Once the program is initiated, these bytes are set in the dump area as in a diagnose instruction.

A separate diagnose instruction is issued to initiate an undump routine and start the suspect microprogram routine at the required step. If the routine comes to a successful conclusion and takes the next sequential instruction, it restarts the loading of the dump area again. This also occurs if the machine check new PSW is ever used (initiated by an error, or loop on ROS), or an external interrupt occurs (from the interrupt key).

The program can be punched into four cards and loaded by the IPL routine.

Operating Instructions

1. Disable the interval timer (if the feature is installed) by using the console key (panel C).

2. Press IPL — this feeds all four cards and the machine goes into the wait state.

3. Switch storage select switch to IC and press the stop key — this should show that bits 4-7 of byte 0 of the storage data register have a hex value of 7.

4. Switch storage select switch to MS and load address 5000 to 501B as shown in the following chart.

This is the dataflow storage area used by the program for data to be used on entry at the required microprogram step:

HEX MS ADDRESS	BYTE 0		BYTE 1	
5000	Blank			YC
5002	YA YB	CPU tag		Skew Reg
5004	Blank	Blank		AX
5006	A0		A1	
5008	Blank		Blank	
500A	D0		D1	
500C	Blank		Blank	
500E	B0		B1	
5010	Blank	Blank		CX
5012	C0		C1	
5014	Blank		Blank	
5016	H		J	
5018	Blank		Blank	
501A			ROAR Bits 7-0	

NOTE: The blank areas are used only to simplify loading a general purpose register before the storage-to-storage transfer into the dump area.

Byte 501A contains the stored stats used in dump/undump. The parity bit of byte 1 gives odd parity of ROAR bits 0-7. The parity bit of byte 0 gives even parity of ROAR bits 8-11. Bit 0 should be used to make odd parity of bits 0-3. Therefore, if ISA, PSA and CPU are all off, the even parity bit (bit 0) must be on to maintain good over-all parity (see byte configuration, Figure 2).

5. When the loading of the data flow storage area is completed, set up the storage data keys for the loop on ROS address as required. Switch to loop on ROS.

6. Press start to return the machine to the wait loop, then press the interrupt key to initiate the program operation.

7. Set CPU check switch to process or disable to avoid stopping on errors.

The program loads to:

HEX MS LOC	HEX DATA					DESCRIPTION
First Card (Col. 1-24)						
0000	00	00	0000	0000	5040	1st PSW used
0008	02	00	5028	4000	0050	1st CCW — read 80 bytes from 2nd card
0010	02	00	0048	0000	0050	2nd CCW — read 80 bytes from 3rd card
Second Card (Col. 1-64)						
5028	80	06	0000	0600	5054	Wait PSW — enabled for Mpx interrupts
5030	01	00	0000			Update LSAR constant
5034	00	00	0004			Update MS constant
5038	01	06	0000	0700	0000	Wait PSW — enabled for external interrupts
5040	48	F0	0052			Load base reg F
5044	41	D0	F200			Load main program address to reg D
5048	40	D0	0052			Store reg D in CCW
504C	9C	00	00XX*			Start I/O CCW used in 0050
5050	82	00	F028			Load wait PSW. Enabled for Mpx interrupt
5054	91	04	0044			Check CSW for device end without errors
5058	47	E0	F050			Return to wait state if condition is not satisfied
505C	58	10	F030			Set up GP reg 1 for later use
5060	58	30	F034			Set up GP reg 3 for later use
5064	82	00	F038			Load wait PSW enabled for external interrupts
Third Card (Col. 1-56)						
0048	00	00	0050			CAW
004C	00	00	0000			Not used
0050	02	00	5000	0000	0050	CCW — data address later modified
0058	01	04	0000	0100	5200	External new PSW

*Input unit address

HEX MS LOC			HEX DATA			DESCRIPTION
0060	01	02	0000	0200	0000	Supervisor call new PSW
0068	01	02	0000	0300	0000	Program check new PSW
0070	01	04	0000	0400	5200	Machine new PSW
0078	01	04	0000	0500	5054	I/O new PSW
Fourth Card (Col. 1-48)						
5200	48	50	F226			Load reg 5 with diagnose constant
5204	18	EF				Load reg E with base address
5206	58	40	F228			Load reg 4 with count (to load dump area 49-4F)
520A	58	00	F22C			Set up reg 0 with LSAR address of undump area
520E	58	20	E000			Load reg 2 from data flow area
5212	83	01	5157			Diagnose instruction to initiate main storage to LSTOR transfer
5216	1A	01				Update LSAR address of undump area
5218	1A	E3				Update MS address of data flow area
521A	46	40	F20E			Branch back unless reg 4 is zero
521E	83	00	500B			Diagnose instruction into suspect routine (undump and process)
5222	47	F0	F200			Unconditional branch back to loop
5226	10	00				Diagnose CPU State constant
5228	00	00	0007			Count constant (to store dump area 49-4F)
522C	49	E5	0000			LSAR address constant

GP registers used in this program:
- GP0 – Used for storage addresses in the storage to storage transfer operation.
- GP1 – Constant used to update LSAR address in GP0.
- GP2 – Used as the data register for transferring MS into the LS undump area.
- GP3 – Constant used to update GPE.
- GP4 – Count register used for looping the required number of times.
- GP5 – Diagnose instruction CPU State constant.
- GPD – Main program start address.
- GPE – Main storage data flow address counter.
- GPF – Base address register.

Codes used in bits 36-39 of the current PSW to determine the source of the PSW:
- 0 = initial IPL PSW
- 1 = External new PSW
- 2 = Supervisor call new PSW
- 3 = Program new PSW
- 4 = Machine check new PSW
- 5 = I/O new PSW
- 6 = Wait PSW for device end without errors
- 7 = Wait PSW for data flow area to be loaded: press interrupt key on completion.

To clear storage with the diagnose instruction on IPL, set Y3 on before entering the following program. This erases all data from the main storage.

If a card is punched to perform a diagnose instruction on an IPL operation, it could be entered before any program being loaded into the machine by an IPL routine. To do this, press IPL twice. Since eight keys must be used to clear MS from the console switch settings, pressing the IPL key twice is much simpler.

The program to perform this operation can be entered into the IPL read area of 24 bytes as shown below:

MS LOCATION HEX	DATA				DESCRIPTION
00	0004	1000	0000	0010	1st PSW – IC pointing to address 10
08	0400	1000	2000	0040	1st CCW – calling sense command
10	4810	000A	8311	100A	Program

The CCW in bytes 08-0F hex has no use. Because of command chaining, the machine forces a CCW. A sense command is issued in this CCW so that no mechanical motion is necessary in the I/O unit. As command chaining is not issued in this CCW, the IPL routine is completed and the 1st PSW is taken from location 00-07. This points the instruction counter to address 10 (the diagnose instruction which sets Y3 and Y7), and enters the microprogram at ROS address (00A). The diagnostic routine is then executed and ends with the microprogram stop lamp on (because the MS location is cleared out and the data expected on the checking run did not appear).

NOTE: Bytes 0001 and 0003 are not cleared.

If IPL is pressed for the second time when this error lamp appears, the program which follows loads normally.

Start at Any ROS Address

This instruction is specified by D2 and B2. It sets stats YA and YB according to R1 and R3 respectively.

Some facilities are provided for this function:

1. Execute dump/undump routine as with the diagnostic control switch on dump position, but by means of programming. The effective address specified by B2-D2 must be 006 and R3 must be set to XXX1 (Y7 on). The microprogram (QS051) initiates a dump routine. At the end of the dump routine it branches on ADR-I condition which is off and goes to undump. After undump, the microprogram returns to next instruction fetch because Y7 is on.

2. Reset errors, set enable, and return to any microprogram address. Effective address (B2, D2)=182 (QS051). The new data flow set up including next ROS address and Y stats setting must be in dump area on exit of this three-microinstruction routine.

This can be used by the diagnostic programmer after a test of error conditions. (Error conditions have been forced into the data flow with the machine in disable state.)

Undump and Process

B2 and D2 must specify ROS address 00B (QS051). Set up data flow according to a pre-determined pattern and start processing at any ROS address determined by the previous setting in local storage dump area. Previous operations can set up the desired data flow pattern, including ROAR, in the dump area in local storage.

The diagnose code sets the inhibit dump latch and transfers to the undump routine. The undump routine loads the data flow from the dump area and starts processing at the ROS address contained in location 15 of the dump area.

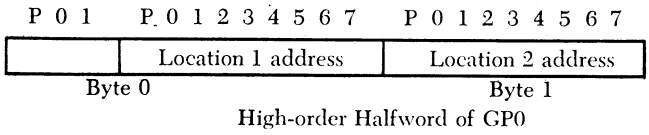
Undump and Execute

B2 and D2 must specify ROS address 610 (QA001). The function is the same as described for undump and process, excepting that the inhibit dump latch is not set before entry to the undump routine.

When the undump signal is given, an error latch is turned on. After the specified microinstruction is executed, the machine enters the error log out routine. There is no other way to initiate a log out by program instruction.

Transfer LS to LS, Compressing

B2, D2 must specify ROS address 157 (QS101). R1-R3, (YA-YB) must be set to 0000 0001. The high-order halfword of GP register 0 must have been previously set up as follows:



High-order Halfword of GP0

The location 1 address (byte 0) refers to any local-storage location that is to be set up (one location of the dump area). The location 2 address (byte 1) refers to the low-order one of a pair of adjacent local-storage locations. (This would normally be a general purpose register, accessible by normal programming).

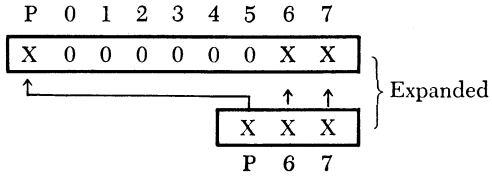
The data is transferred as follows:

The low-order halfword of the general-purpose register specified at location 2 address is transferred into bytes 0 and 1 of location 1. Byte 1 of the high-order halfword of the general-purpose register specified at location 2 address is compressed and transferred into byte X of location 1.

Transfer LS to LS, Expanding

This is the reverse of the previous operation. The setting of the YA and YB stats (0000 0011) selects a different microprogram path. The effective address of the diagnose instruction still indicates the same starting point, 157 (QS101). Location 1 and 2 addresses are set up as before in the general-purpose register 0 high-order halfword.

In this case the transfer is from location 1 to location 2, expanding instead of compressing:



Clear a Local Storage Location

The R3 field in the instruction = 1X01 and effective address B2, D2 = 157 (QS181). The address of the location to be cleared must be loaded into general-purpose register 0, in the location 1 address. This location is left in the readout state.

Transfer a Data Halfword from Local Storage to Multiplex Storage

The R1 and R3 field of the instruction = X1XX1000 and effective address B2, D2 = 157 (QS181). The multiplex storage address must be previously loaded into general-purpose register 0, high-order halfword.

The pattern to be transferred must be previously loaded into general-purpose register 0, low-order halfword.

The diagnose instruction transfers the data halfword from the low-order half of general-purpose register 0 to the specified multiplex storage location.

Transfer a Data Halfword from Multiplex Storage to Local Storage

The R1 and R3 field of the instruction = X1XX 0000 and effective address B2-D2 = 157 (QS101). The multiplex storage address must be previously loaded into general-purpose register 0, high-order halfword. The diagnose transfers the data halfword from the specified multiplex storage location to general-purpose register 0, low-order part.

Cycle a Multiplex Storage Word Under Worst Case Noise Conditions

The R1 and R3 field of the instruction = X1XX 0010 and effective address B2-D2 = 157 (QS101). The multiplex storage address must be previously loaded into general-purpose register 0, high-order halfword. The bit patterns must be loaded into the write locations of general-purpose registers 1 and 2 as shown in the following table:

	P 6 7 P 0 7 P 0 7	
GP Reg 0	Bump Location Address	
	Worst Case Bit Pattern	Read Loc 1
GP Reg 1	Complement Worst Case Bit Pattern	Write Loc 1
	Complement Worst Case Bit Pattern	Read Loc 2
GP Reg 2	Worst Case Bit Pattern	Write Loc 2
	Not Used	

The worst case bit pattern must be loaded into the multiplex storage location to be cycled before calling the diagnose instruction.

The diagnose instruction reads the multiplex storage location into read location 1 (worst case), writes from write location 1 (complement worst case), reads into read location 2 (complement worst case) and writes from write location 2 (worst case), then exits from diagnose to I-fetch. An unconditional branch back to the diagnose instruction would cycle this routine continuously.

Cycle a Storage Protect Local Storage Word Under Worst-Case Noise Conditions

For that part of SPLS allocated to CPU the R1 and R3 field of the instruction = 00XX 0110 and the effective address = 157 (QS101). For that part of SPLS allocated to the multiplex channel, the R1 and R3 field = 01XX 0110 with the same effective address.

The main storage or multiplex storage address associated with the storage protect word to be operated on must be loaded previously into general-purpose register 0, high-order halfword.

The bit patterns must be loaded into the write locations of general-purpose registers 1 and 2 as shown in the following table:

	P 6 7 P 0 7 P 0 7			
	Address of SPLS Location			
GP Reg 0	Worst Case Bit Pattern	SPLS	CPU Channel	Read Loc 1
	Complement Worst Case Bit Pattern	↑	↑	Write Loc 1
GP Reg 1	Complement Worst Case Bit Pattern	↓	↓	Read Loc 2
GP Reg 2	Worst Case Bit Pattern	DATA	KEY	Write Loc 2
	Not Used			

The worst case bit pattern must be previously written in the specified storage protect location. The diagnose instruction reads the storage protect word into read location 1, re-writes from write location 1, re-reads into read location 2 and re-writes from write location 2.

Read Only Storage (ROS)

A MAP (Figure 911, *System/360 Model 40 2040 Processing Unit, Field Engineering Diagrams Manual,* Form 223-2842) is provided to locate faults in ROS quickly. This chart indicates a procedure which quickly detects the failing area, and provides diagnostic evidence for repairs. Complex or multiple errors requiring special test equipment are not covered in the chart, but most errors can be located rapidly.

When a ROS fault is suspected, note all relevant machine status before starting the MAP procedure. This prevents the loss of valuable diagnostic information if the fault is not in the suspected area. If the machine is in a hardstop condition, status can be noted from the indicators. Otherwise, consult the log out information.

ROS Display

These ROS conditions are displayed on the console and internal CE panel:

1. ROBAR is directly displayed on the operator's console panel and contains the address of the word last executed.
2. ROAR may be displayed in hardstop on the R bus lights. It contains the address of the word to be executed.
3. The word in the sense latches is displayed directly on the internal CE panel. This word is normally associated with the address in ROAR, but when an early or control check is encountered, the inhibit signals generated cause the sense latches to hold the word associated with the address in ROBAR.

ROS Diagnostic Aids

There are three special "words" in ROS for fault finding. These words are:

1. A word containing all 1's is at address 020. Calling this word gives wrong address parity and wrong word parity.
2. A word containing all 0's is at address 010. Calling this word gives correct address parity, but wrong word parity.
3. A word to force ROS data checks is located at 05A.

By manually selecting these words, a solid ROS data error can be easily recognized.

Isolating an Array Diode Short-Circuit

When an array diode short-circuit is suspected, isolation to half a module can be obtained by removing, one at a time, then replacing, the C and Z connectors (two per module) of the unselected modules.

When the connector feeding the failing component is removed, a correct pattern is obtained from the error word.

If the fault has not been isolated when all unselected modules have been tried, the fault is in the selected module. Addressing a word in another module as the test word enables diagnosis to half a module.

Having isolated the fault to half a module, all I/O connector cards should be plugged in and an error word selected. Initiate repeat-on-ROS for scoping. A check at the output pins of the 32 drivers feeding the half module in error shows one line with a higher positive potential than all others (not including the selected driver). This is the drive line feeding the error diode.

Selecting the drive line feeding the error diode, which is combined with the four gates of the error module, results in one combination that gives a correct word pattern output. This correct word is the one associated with the diode with the short circuit. The failing component may be located and replaced on the diode board layout.

Loop on ROS

If the looped address is in CPU checkout, system reset, or load microprogram routines, a new machine check PSW in location 70 hex is unnecessary.

Stop on ROS

It is impossible to stop on a ROS address following any hardware cycle; i.e., the first cycle of CPU checkout, because the address compare occurs at T4 before the address set in the data keys and, in these cases, the T clock has been stopped.

Determining Next ROS Address

See Figure 3.

Microprogram Test Conditions

In the formation of the next ROS address, the B and C conditions can be altered in the cycle when they are tested.

IDQ and IZT: IDQ and IZT (invalid decimal digit on the Q bus and integrated zero test) are tested on the result of the operation carried out in the present cycle with any result which has occurred since the latched conditions were previously reset. The reset may be from the CN field or as a result of testing the conditions; i.e., a reset occurs after testing for the condition.

Staticizers Y0-Y7: These conditions may be tested in the next cycle after they are set up, or later. If they are tested in a cycle in which they are changing, either by means of the ALU operation or the CE field, the result is based on their old values.

Carry Stats YCI and YCD: Conditions tested depend on the results of the operation occurring in the cycle or since the ALU last operated in a similar mode (indirect or direct). SAT may be the result of ISA, PSA and YM stat. In the first case, SAT can be tested on the result of calling storage in that cycle, since reset of ISA occurs early in the cycle when the next read call is given. Thus, the set is a result of the new condition.

PSA: PSA may be tested in the cycle after the read call is given. The YM stat (Y0) must be set in a cycle before the testing cycle.

PRI (Program Interrupt): This condition is tested early in a cycle but changes late in a cycle. Thus the condition depends on occurrences in previous cycles.

Logic Locations of ROS Control Fields

See Figure 4.

Machine Stops on ROBAR Address (Junction Point of Several Microprogram Routines)

Check the Y stat settings to see which microprogram routine caused the stats to be set. Use Figure 3.1 to locate the correct CAS block.

Stopping on PSA or ISA Condition

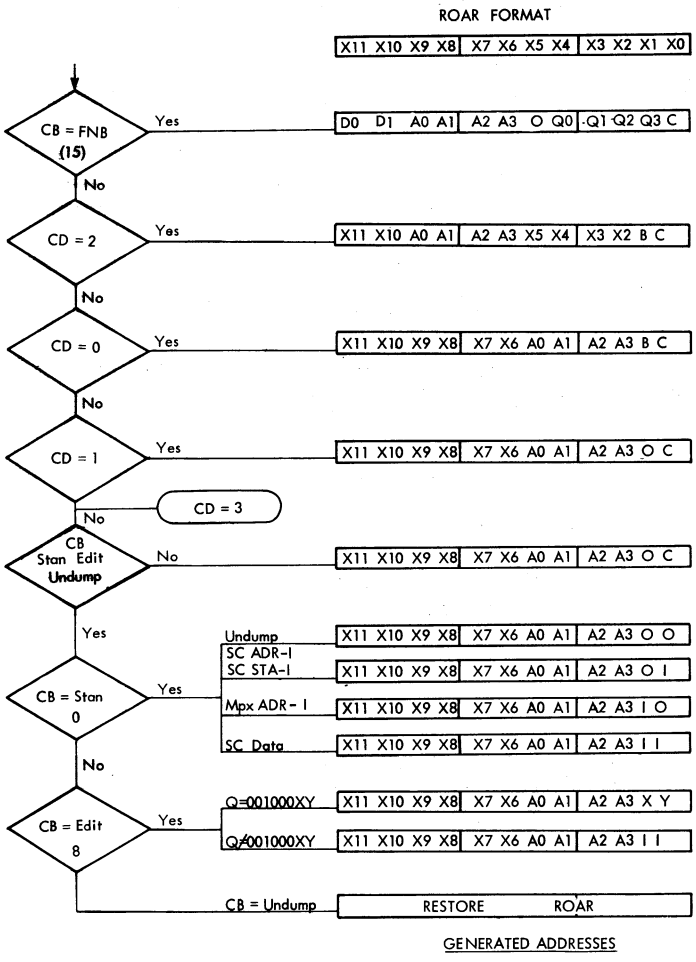
The PSA or ISA condition is always presented to the program either as an interrupt or in the status byte. The best way to determine exactly when the condition occurs is to stop ROS on 431 (QC021), that is in the trap routine microprogram which follows immediately on detection of the condition.

ROS Data Checks

ROS data checks can be caused by addressing failures that affect the duration and level of the TROS drive current. These checks cause picking or dropping of bits because of the wrong word being addressed for part of the drive cycle. Frequently, the next address set up is wrong, but resembles what it should have been. To check this condition, sync the scope on the last correctly read word and check the driver pulse at the TROS board. The duration of the pulse should be 180 ns. If ROS data checks are caused by late addressing, repeat on ROS does not show up the fault.

Intermittent faults (picking or dropping of bits) may be caused by:

1. Unpunched bit position on ROS tape.
2. Using the wrong stagger tape.
3. Timing.



NOTES

A0 A1 A2 A3 = CA Field
B = B Condition *
C = C Condition **
D0 D1 = CD Field
Q0 Q1 Q2 Q3 = MS Bits Of Q Bus
X Y = Bits 6 & 7 Of Q Bus
X11 X10 etc = Old ROAR Bits

* Bit One of ROAR is set to '1' if the condition specified by the CB field is satisfied or if the CB field = 01, and set to '0' if the condition is not satisfied or the CB field = 00.

** Bit zero of ROAR is set to '1' if the condition specified by the CC field is satisfied or if the CC field = 01, and set to '0' if the condition is not satisfied or the CC field =00

Stan { CD = 3, CB = 0
Edit { CD = 3, CB = 8
Undump { CD = 3, CB = E

001	Dump
002	Diagnostic Control Switch - MS Validate
003	Dump 2nd Level
005	System Reset: Load Button: Diagnostic Control Switch - CPU
006	Diagnostic Control Switch - Dump
009	Diagnostic Control Switch - MS Pattern
00A	Diagnostic Control Switch - MS Address
00C	Diagnostic Control Switch - LS Pattern
00D	Diagnostic Control Switch - LS Address
400	Start Button
402	Display Button
403	Store Button
404	Trap During Read Phase
405	Trap During Write Phase

Figure 3. Determine Next ROS Address

	Type of Check			
	Early (Except LS Read)	Control	Late	Local * Storage Read (Early)
Error detected in microinstruction	A	A	A	A
ROBAR indicates microinstruction	A	A	A	B
ROAR indicates microinstruction	B	B	B	C
Sense latches set by microinstruction	A	A	B	B

*MS protect key, MS protect data register, and stat checks give same indication as local storage read.

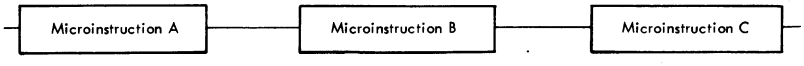


Figure 3.1. Microinstruction Status on Hardstop

ROS Bit	SENSE LATCH Connector Gate	Board	Socket	Pin	CONTROL Field	Bit	FUNCTION
0	A	A2	A5	B2	A	0	ROS Next Address
1	A	A2	A5	D2	A	1	
2	A	A2	A5	B3	A	2	
3	A	A2	A5	B4	A	3	
4	A	A2	A5	D4	B	0	B Condition Tests, Special Controls
5	A	A2	A5	B5	B	1	
6	A	A2	A5	D5	B	2	
7	A	A2	A5	D6	B	3	
8	A	A2	A5	B7	C	0	C Condition Tests
9	A	A2	A5	D7	C	1	
10	A	A2	A5	B8	C	2	
11	A	A2	A5	B9	C	3	
12	A	A2	A5	D9	D	0	ROS Address Control
13	A	A2	A5	B10	D	1	
14	A	A2	A5	D10	E	0	Emit Field
15	A	A2	A5	D11	E	1	
16	A	A2	A5	B12	E	2	
17	A	A2	A5	D12	E	3	
18	A	A2	A5	B13	F	0	Word Address Parity
19	A	A2	A5	D13	G	0	ALU Function Control
20	A	B2	A3	B2	G	1	
21	A	B2	A3	D2	H	0	Local Storage Address Control
22	A	B2	A3	B3	H	1	
23	A	B2	A3	B4	H	2	
24	A	B2	A3	D4	H	3	
25	A	B2	A3	B5	H	4	
26	A	B2	A3	D5	J	0	R Bus Input Control
27	A	B2	A3	D6	J	1	
28	A	B2	A3	B7	J	2	
29	A	B2	A3	D7	K	0	Skew Control of ALU Q Bus Entry
30	A	B2	A3	B8	L	0	R Bus Output Control
31	A	B2	A3	B9	L	1	
32	A	B2	A3	D9	L	2	
33	A	B2	A3	B10	M	0	ALU Output Control
34	A	B2	A3	D10	M	1	
35	A	B2	A3	D11	M	2	
36	A	B2	A3	B12	M	3	
37	A	B2	A3	D12	N	0	CE Field Stat Control
38	A	B2	A3	B13	N	1	
39	A	B2	A3	D13	N	2	
40	A	B2	A4	B2	N	3	
41	A	B2	A4	D2	P	0	ALU Input from P Bus
42	A	B2	A4	B3	P	1	
43	A	B2	A4	B4	P	2	
44	A	B2	A4	D4	Q	0	ALU Input from Q Bus
45	A	B2	A4	B5	Q	1	
46	A	B2	A4	D5	Q	2	
47	A	B2	A4	D6	Q	3	
48	A	B2	A4	B7	R	0	Miscellaneous
49	A	B2	A4	D7	R	1	
50	A	B2	A4	B8	R	2	
51	A	B2	A4	B9	S	0	Word Parity Bit
52	A	B2	A4	D9	T	0	Carry Control
53	A	B2	A4	B10	T	1	
54	A	B2	B8	E04	J	X	R Bus Input Control
55	A	B2	B8	B04	P	X	ALU Input from P Bus

Bit Number	0				1								2								3								4								5					
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5
Field	CA			CB			CC			CD	CE				CF	CG	CH				CJ			CK	CL			CM			CN			CP		CQ			CR			CS	CT	CJ	CP
Bit Value	8	4	2	1	8	4	2	1	8	4	2	1	2	1	8	4	2	1	1	2	1	6	8	4	2	1	1	4	2	1	8	4	2	1	4	2	1	8	4	2	1	4	2	1	1	2	1	8	8
Control: Data Flow											CE					CG	CH							CK	CL			CM			CN			CP		CQ			CR				CT	CJ	CP
Special	CA			CB			CC			CD																													CR							
ROAR				CB																																										
Parity															C F																									C S						

Figure 4. ROS Control Word and Basic Functions

Main Storage

Clearing Main Storage to Zeros

Main storage is set to zeros if stat Y3 is set before starting the address test diagnostic. This causes a microprogram stop.

Determining Incorrect Parity Words in Main Storage

Incorrect parity words in main storage are found by running the main storage validate internal diagnostic while the CPU check switch is in error/stop mode. Any incorrect parity word causes the machine to stop. Correct parity is written automatically in the memory system reset. Start procedure should keep checking the memory in ascending order from address 00000.

The status of main storage may be checked while running a program. Stop the system with the stop pushbutton, allowing all I/O operation time to complete. Turn the diagnostic control switch to main storage validate. Run the diagnostic. This puts the machine in hardstop if bad main storage parity is found. To restart the main program: reset the system, set the diagnostic control to off and press start. The instruction count in the PSW should restart the program at the point where it stopped.

Main Storage External Worst Case Diagnostics

Externally loaded main storage worst case diagnostics do not use the lower portion of main storage (PSW's area, etc.). This section is used by the ROS stored (internal) worst case diagnostics.

Results of Main Storage Parity Error

The time during the R/W cycle that the parity error occurs is important. In some cases the storage area may be left blank. Figure 5 summarizes these conditions.

		Main Storage Check	
Occurs During		Parity check in the MS register (A) or (D)	Result in Main Store
Read Phase	Cycle 1	Stop T clock at end of current cycle (T4) Read function continues to completion Read latch remains ON +	The location specified by register A is left read-out *
	Cycle 2	Stop T clock at end of current cycle (T4) Read function completed Read latch remains ON +	The location specified by register A is left read-out *
	Cycles 3,4,5	Stop T clock at end of current cycle (T4) Read latch remains ON +	The location initially specified by register A is left read-out *
Write Phase	Cycle 1	Stop T clock at end of current cycle (T4) Write function continues to completion	The location initially specified by A may be left read-out * The location specified by changed A may hold bad data **
	Cycle 2	Stop T clock at end of current cycle (T4) Write function completed	The location initially specified by A may be left read-out The location specified by changed A may hold bad data **

* Any MS location in a read-out condition has bad parity.
\+ If system reset is called and the read latch is On, an MS write operation is forced.
** Writing into an uncleared location will OR the old and new data, giving bad data and probably bad parity.

Figure 5. Main Storage Check

Local Storage

Figure 6 shows the contents of local storage and the addresses of the registers in it.

Channel Diagnostic Techniques

Abbreviations for Channel

ADR-I	Address in
ADR-O	Address out
CAW	Channel address word
CCW	Channel control word
Chán	Channel
CMD-O	Command out
Ctrl	Control
HIO	Halt input/output
ICC	Interface control check
IF	Interface
I/O	Input/output
IR	Interrupt request
Mpx	Multiplex
PRI	Program interrupt
Req in	Request in
SC	Selector channel
Sel in	Select in
Sel out	Select out
SIO	Start input/output
STA-I	Status in
SVC-I	Service in
SVC-O	Service out
TIC	Transfer in channel
UCW	Unit control word

Channel fault-finding techniques are described in the channel MAP's (Figure 665 through 675 in the *System/360 Model 40 2040 Processing Unit Field Engineering Diagrams Manual,* Form 223-2842). These MAP's are supported by the ECAD's. This section explains some of the areas not covered by MAP's and ECAD's.

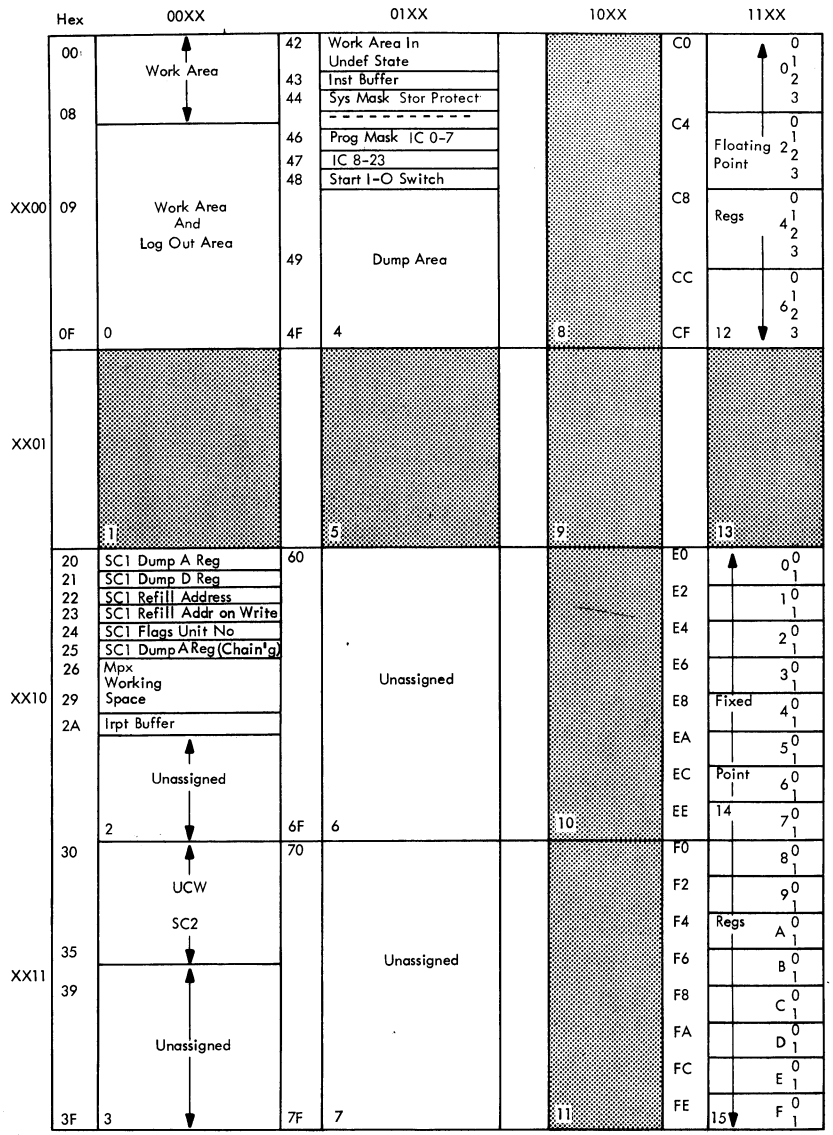


Figure 6. Local Storage Contents and Address

	Reg Number	LSAR Address (Hex) Display in Hard Stop	Console Display Address (Hex) (Set in A1 Byte of Storage Address Keys)
General Purpose Registers	0	E0 - E1	00 - 01
	1	E2 - E3	10 - 11
	2	E4 - E5	20 - 21
	3	E6 - E7	30 - 31
	4	E8 - E9	40 - 41
	5	EA - EB	50 - 51
	6	EC - ED	60 - 61
	7	EE - EF	70 - 71
	8	F0 - F1	80 - 81
	9	F2 - F3	90 - 91
	10 (A)	F4 - F5	A0 - A1
	11 (B)	F6 - F7	B0 - B1
	12 (C)	F8 - F9	C0 - C1
	13 (D)	FA - FB	D0 - D1
	14 (E)	FC - FD	E0 - E1
	15 (F)	FE - FF	F0 - F1
Floating Point Registers	0	C0 - C3	00 - 03
	2	C4 - C7	20 - 23
	4	C8 - CB	40 - 43
	6	CC - CF	60 - 63

MPX Chan

IF Tag	IF Control	IF Parity	Channel Data	Channel Control (Only during Mpx Data Service)	Cause of Error
X X	X X			X	More than one in or out tag. Or tag sequence check during data or during selection.
	X X			X	Time out, unit failed to respond in time or raised an incorrect tag during data service or during select ICC. (See ROBAR list under "Interface Control Check.")
	X	X		X	Parity check on Bus In caused by address in or status in.
	X	X			Parity check on Bus In caused by address in or status in during initial selection.
			X		Parity check on bus in caused by service in.
				X	Any CPU check occurring while the microprogram and data flow are being used as a Mpx channel.
		X			Parity check on Mpx interface register during ADR-O, CMD-O (during selection).
		X		X	Parity check on Mpx interface register during data service ADR-O, CMD-O, SVC-O.

Figure 7. Error Check Combination for Multiplex Channel Operations

Multiplex Channel Errors

I/O Device Errors

I/O devices are equipped with their own check circuits according to the type of device. Unless the faults interfere with the interface, the channel detects the faulty condition by an indication in the status byte. More information is provided to the channel in the sense byte.

Interface Tag Check

A check is performed on the six interface tags so that not more than one inbound tag and not more than one outbound tag is on at any one time. This check is made every cycle at T2.

Interface tag check is also brought on by the tag sequence check. The tag sequence check ensures that the in tag rises before the out tag, and that the in tag falls before the out tag.

Interface Control Check

A microprogram time-out loop detects the failure of a control unit to respond with the correct tag within the allowed time. This is done by testing for the rise or fall of a particular tag and incrementing a count. If the wrong tag rises, it appears to the microprogram that the control unit failed to respond. When the time-out occurs, interface control check is set by ICC(CD = 1, CB = 10). Interface control check is also set by interface tag check at T2, or by a parity check on bus in at T3 when an address in or status in tag is on; the microprogram calls for a transfer from bus in to the R register. Determine which error condition set the interface control check by examining the other check indicators (Figure 7). The four conditions which cause the ICC are:

1. Interface tag check
2. Address in tag up and a bus in check
3. Status in tag up and a bus in check
4. Microprogram set ICC(CD = 1, CB = 10)

Interface Parity Check

Bus in parity is checked at T3 of any cycle in which an inbound tag is on and the microprogram calls for a transfer from bus in to the interface register. Correct parity is generated when transferring to the R register.

All adapters and devices force correct parity on transmitted data.

Channel Data Check

Channel data check is set when a parity check occurs on bus in and the service in tag is on. The check is made at T3 of the cycle in which bus in is transferred to the R register.

Unit Serviced at Time of Fault (Multiplex Channel)

Unless the fault prevents it, the unit number of the device being serviced is in LS location 28. Working from a log out, the bus in unit number is in the MS log out area location 0108, byte 1. See Figure 8.

Op Code and Flags (Multiplex Channel)

These are found normally in LS location 29. Note, however, that this depends on where the microprogram is. During the IPL initial selection, the CCW count

Sel. Chan

SC1 Channel Check Indicators

Display Roller Position 2 (Channel Select to SC1)								Console Panel "A"		
T0	T1	W0	Bus In	CCW Flags	IF Tag	IF Ctrl	Channel Control	SC1	Late	Type of Check
X							X	X	X	T0 Parity Check
	X						X	X	X	T1 Parity Check
		X					X †	X	X	W0 Parity Check on Data Service
		X				X	X †	X	X	W0 Parity Check Not Data Service
			X			X	X †	X	X	Bus In Parity Check, Not Data Service
				X			X	X	X	Flag Parity Check
					X	X	X †	X	X	Multiple Tag Check, In Tags
					X		X	X	X	Multiple Tag Check, Out Tags
						X	X †	X	X	ICC - Time Out, Addr, Non-Compare, Etc.
										(See ROBAR list under "Interface Ctrl Check.")
							X †	X	X	CPU Control or Late Check } With Start Latch or Channel Sel Late
							X †	X		CPU Early Check } With Start Latch or Channel Sel Late
← Any Check →								X	X	Channel Check and Not Start Latch
Display of Checked Data	Display Roller to Position 5 Channel Display to T0, T1 Channel Select to SC1	Display Roller to Position 5 Channel Display to T0, T1 Channel Select to SC1	Display Roller to Position 5 Channel Display to W0, W1 Channel Select to SC1	Display Roller to Position 5 Channel Display to W3, W4 * Channel Select To SC1	Display Roller to Position 4 Channel Select to SC1	Display Roller to Position 3 Channel Select to SC1	Display Roller Position 2 and 3 Channel Select to SC1	All CPU and Channel Checks	All CPU and Channel Checks	All CPU and Channel Checks

† Channel Control Check Latch Set by CPU Check (Master Check Latch).

* Bus in data bits may be displayed from W4 but the associated parity bit will then be a generated parity bit.

Figure 8. Channel Check Indicators

is stored in this location until the initial status is accepted by the service out.

The five check latches used in combination can aid in fault analysis. See Figure 7.

Selector Channel Errors

Interface Tag Check

A check is made on SVC-I, STA-I, ADR-O, ADR-I, SVC-O and CMD-O so that there is no more than one inbound tag and one outbound tag on at any one time. Interface tag check also sets ICC for an in tag error or checks for an out tag error.

Interface Control Check

This check is set by the microprogram as in the multiplex channel.

It is set by multiple-in tags when the multiple tag check is set. It is set by interface parity error during selection or status. It is set by a W0 parity error during data service for write.

Interface Parity Check

Parity of the interface is checked for all transfers of data or control information. W0 is parity-checked for outbound tags and bus in is parity-checked for inbound tags. Correct parity is always forced into W4.

Channel Data Check

Channel data check is forced for incorrect interface parity during data service.

Channel Control Check, Multiplex and Selector Channels

Channel control check latch is set by any of the channel error check latches. It will also be set by any CPU check condition when the CPU is running in multiplex I/O mode.

If the CPU is running in error-check disable mode and encounters an error, the channel control check latch is set if the channel is selected. This may give the false impression that the fault occurred as a result of a failure in the channel. See Figure 7.

Interface Control Check (ICC)

The following table lists ROBAR addresses and conditions which bring on the ICC latch.

ROBAR	CAS PAGE	REASON
567	QB141 (20us)	Time-out because of service out or command out taking excess time to drop. Also op in and no ADR-I or STA-I gives this condition. This happens only during command chaining (Mpx).
58B	QB161 (40us)	Unit takes excess time to complete initial selection (Mpx).
59D	QB551	Device waiting to interrupt did not reply to selection.
5D6	QB121	If unit responds with sel in to address out, unit unobtainable. On command chaining, ICC is set (Mpx).
5E5	QB121 (81us)	If Y4 is off, time-out because unit takes excess time to drop req in or sel in (Mpx).
5E5	QB121 (60us)	If Y4 is on, time-out because of unit taking excess time to reply to ADR-O, or unit raising other than ADR-I or STA-I (Mpx).
5F5	QB121	Address on bus in in reply to ADR-O does not match address sent on bus out (Mpx).
5F7	QB121	Same as above, but on command chaining (Mpx).
5FD	QB151 (40us)	Device takes too long to present status (Mpx).
619	QA011	15A on UCW address (Mpx).
653	QA091	Y4 on. Time-out caused by OPI taking too long to drop after issuing unit with CMD-O to SVC-I (Mpx).
653	QA091	Y4 off. Time-out caused by SVC-I OPI taking too long to drop after issuing unit with SVC-O (Mpx).
65F	QA131	Y4 on. Time-out caused by SVC-I OPI taking too long to drop after command out to stop (Mpx).
6BF	QA231 (80us)	Time-out because of SVC-O or CMD-O taking too long to drop (Mpx).
726	QB541	ICC because address on bus in does not match address sent on bus out (SC).
776	QB501	Time-out; interface free takes too long (SC).
786	QB211	Unit takes excess time to reply with STA-I when it issues command out.
7A6	QB211	Unit takes excess time to complete initial selection.
7A7	QB551	Invalid interface response (SC).
7AB	QB461	Unit takes excess time to drop op in when issued with halt I/O (SC).
7BB	QB551	If address out up, time-out because of no ADR-I in time. If address out not up, time-out because of unit taking excess time to reply to command out. Should be status in (SC).
7C6	QB231	Unit takes excess time to drop SVC-O command out on halt I/O.
7D7	QB521 (80us)	Op in takes too long to fall (SC).

Faults Detected by Microprogram

The load routine tests for various error conditions only when loading. The error indication is load light ON and the CPU in one of these continuous loops:

ROBAR	CAS PAGE	ERROR CONDITION
50D	QB101	Trying to load from a non-existent channel. Check load unit switches.
4F6	QC121	Waiting for channel end interrupt from the selected device.
4FB	QC111	Channel status byte (in B1) contains an invalid bit. Only the PCI is allowed.
4CB 4F8	QC111	1. No channel end bit in the final status byte (unit status is in B0, channel status in B1). 2. If channel end is present initially, a further test is carried out one step later at 4F9. If any bits other than status modifier, channel end or device end are present, microprogram loops back to 4FB.
596	QB191	Unit A Unit Unavailable

I/O Program Checks

The conditions that give this check are:

1. Bits 5-7 of ALU output non-zero during loading of channel flags
2. ISA detected during Read or Write but not Skip
3. Bits 4-7 of CAW are non-zero
4. Command specified in CCW invalid
5. CCW address not on double word boundary (low order four bits must be zero)
6. Count in CCW is zero
7. Bits 37-39 of CCW are not zero unless CCW specifies a TIC
8. First CCW fetched specifies a TIC or two TIC CCW's in succession.

All of the above cause termination of I/O operation; CSW is stored with program check bit on.

Common Interface Responses

INTERFACE SIGNALS	FUNCTION
Service out to status in	Accept the unit status
Command out (zero byte) to status in	Stack the unit status in the device
Command out (zero byte) to service in	Stop the data transfer
Command out (command byte) to address in during initial selection	Send command to the device on the bus out
Command out (zero byte) to address in	Proceed with data service
Service out to service in	Normal channel response to the device during data service
Suppress out and service out to status in	Command chaining is in progress
Status in to address out	Control unit busy
Select out down	Interface disconnect
Address out up Operational in up	The device removes all signals from the interface but obtains re-selection to present status after reaching its normal ending point
Suppress out up Operational out down	Selective reset: unit on interface stops at normal stopping point and its status is reset
Operational out down Suppress out down	System reset

Initial Selection With No Interrupts Stacked (Multiplex or Selector Channel)

CHANNEL	DEVICE	
Select Inhib sel out		Microprogram set req in, sel in select } Interface free timeout if IF delayed too long
ADR-O		To all units on channel only one should reply
Sel out Hold out		Set by fall of microprogram ADR-O; (delayed 400 nanoseconds behind ADR-O).
	Op in ADR-I	In after ADR-I address byte will be in interface register. Time-out if ADR-I delayed too long.
CMD-O		Issue command from CCW, shown in interface register
	STA-I	Should be zero status
SVC-O		I/O device starts mechanical motion. Time-out if SVC-O stays up too long.

Mpx Data Service

CHANNEL	DEVICE	
	Req in	
Sel out and hold out		
	OPI	
	ADR-I	Causes CPU to dump. Then scan indicates multiplex channel requires service. Fetch UCW for command data address and count.
CMD-O		Zero command byte on IF indicates proceed.
	SVC-I	Indicates multiplex data service.
SVC-O		Indicates byte accepted on read. Indicates byte ready on IF for write. Reset by fall of SVC-I, indicating device has accepted byte on write. Update UCW and replace in multiplex storage scan to undump if no other multiplex unit requires service.

Mpx Status In

The channel end, device end condition is present when a device ends operation. The status byte is stored in the CPU (UCW) and causes an I/O interrupt. Then PSW is masked to allow the multiplex channel to function as follows:

CHANNEL	DEVICE	
	Req in	
Sel out and hold out		
	Op in	
	ADR-I	Causes CPU to dump. Then scan indicates multiplex channel requires service. Fetch UCW.
CMD-O		Zero command byte on IF indicates proceed.
	STR-I	Indicates device ending. Check for channel end and any other status bits including device end. If channel end with or without device end, test IR; if IR off, set it. Set interrupt buffer with channel end bit. Set maskable interrupt stat which forces PRI on next I-Fetch. Update UCW with status.
SVC-O		Indicates status has been accepted by channel. Scan and undump CPU unless another multiplex unit requires service.

I/O Interrupt Caused by Channel End, Device End, Stacked in CPU (UCW)

CHANNEL	DEVICE	
		PRI forces branch to test multiplex IR. This indicates multiplex interrupt. Check interrupt buffer for end (2) bit. End (2) bit indicates status stored in UCW. Reset IR. Reset MI and inhibit dump stat.
Inhibit sel out		Fetch UCW. Load CSW from UCW. Store I/O old PSW. Load I/O new PSW.

1401/1460 Compatibility Feature

Special checking is provided for machines with the 1401 compatibility feature.

1. The 13-bit ROS address is parity-checked.
2. The output of the 1401 address translator is parity-checked.
3. The output of the selector-channel data-in translator is parity checked.
4. The added ROS controls are parity-checked.

ROS Address Parity Checking

The ROS address check latch is set if parity of ROSAB and the 13th ROS address bit are not equivalent to bit 18 of the associated ROS word.

Main Storage Address Checking

A parity error in the translated 1401 address is indicated as a main storage address error (MS ADR).

An invalid 1401/1460 address character may be decoded into a hexadecimal character and placed in one of the three decimal (DDD) positions of the address register. A main storage address check (MS ADR) occurs even though the address register has correct parity. The 1401 address translator cannot handle hexadecimal characters in the decimal positions. If a MS ADR check occurs and main storage address register parity is correct, check ROAR bit 12. If ROAR bit 12 is on (1401 mode), check the three rightmost positions of the main storage address register. These three positions should be decimal characters.

Selector Channel Data Checking

Transmission of data from the I/O interface to the selector channel data translator includes parity, but parity is not used to check data at the translator. The transmission of translated data from the translator to the System/360 Model 40 W register is parity-checked. A not check condition causes a "bus in parity error" which sets "channel data check" bit in the CSW.

The transmission of data from the System/360 Model 40 W0 buffer to the selector channel data translator (write tape operations) include parity, but the parity is checked in the selector channel control unit.

ROS Field Checks

The functions CB = 9 or CB = 10 are included in the B field decoder check. The function CC = 6 is included in the C field decoder check. The function CN = 13 is included in the N field decoder check. If no Relocate latch is set, an addressing exception interrupt results.

Diagnostic Programs

The following diagnostic programs test the 1401/1460 compatibility feature (without Relocate):

IDENTIFICATION	LOADER	PART NO.	DESCRIPTION
4F01	DMK	5396027	Hardware Test
4F02	DMK	5396030	Hardware Test
4F03	DMK	5396033	Hardware Test
4F04	DMK	5395902	I/O Hardware Test (1401 Language)
4F05	DMK	5396264	Hardware Test

The following diagnostic programs test the 1401/1460 compatibility feature (with Relocate):

IDENTIFICATION	PART NO.
4F09	5448693
4F11	5448701
4F16	5487384
4F17	5487387
4F18	5487390
4F1A	5487393
4F1C	5487396

Additional information concerning the 1401/1460 compatibility feature may be found in the *System/360 Model 40, 1401/1460 Compatibility Feature, Field Engineering Theory of Operation,* Form Y22-2859.

1401/1440/1460 DOS Compatibility Feature

The following diagnostic programs test the 1401/1440/1460 DOS compatibility feature for the 2040. All diagnostics except 4F0C are revisions of diagnostic programs for the 1401/1460 compatibility feature.

IDENTIFICATION	LOADER	PART NO.	DESCRIPTION
4F06	DMK	5448684	Revision of 4F01
4F07	DMK	5448687	Revision of 4F02
4F08	DMK	5448690	Revision of 4F03
4F09	DOS	5448693	Revision of 4F04
4F11	DOS	5448701	Revision of 4F04
4F0A	DMK	5448696	Revision of 4F05
4F0C	DMK	5448699	Feature Hardware Test

Additional information about the 1401/1440/1460 DOS compatibility feature may be found in the following manuals:

System/360 Model 40, 1401/1460 Compatibility Feature, Field Engineering Theory of Operation, Form Y22-2859.

System/360 Model 40, 2040 Processing Unit, Field Engineering Diagram Manual, Form Y22-2842.

1410/7010 Compatibility Feature

Installation of the 1410/7010 compatibility feature provides the system with the following additional checks:

1. The 1410 address translator output is parity checked.
2. The 13-bit ROS address is parity checked.
3. Additional ROS micro-orders are parity checked.
4. Invalid 1410 characters are detected.
5. Selector channel data-in translator is parity checked.

Main Storage Address Check (MS ADR)

A parity error in a translated 1410 address causes a main storage address error.

Addresses over 80K are normally invalid in emulated 1410 object programs; however, addresses between 80K and 100K are handled as data by the compatibility feature:

1. When the address after indexing is between 80K and 100K
2. When a clear storage operation wraps around storage at address 00000
3. On a store address register operation

If an address over 80K is used to address main storage, a MS ADR check may or may not occur, depending on the bit combination.

ROS Address Bus Parity Check (ROS ADR)

Bit 12 is added to ROAR to address the additional 1410 compatibility microprograms in ROS. ROSAB parity (bit 13) is compared to the CF field of the associated ROS word. An unequal comparison sets the ROS address check latch.

ROS Data Parity Check (ROS DATA)

The following micro-orders are added to the ROS data parity check by the 1410 compatibility feature:

DECIMAL ORDER	MICRO ORDER	
CB = 9	SMSC	Set 1410 emulator control latches on selector channel.
CB = 10	DAT	Disable decimal address translator.
CC = 6	MSC	Test emulator mode latch.
CN = 14	0110,DSPN	Set numeric mode latch, set function register equal to emit field.
CT = 1	M	Extend ROS address.

Additional micro-orders are changed in their function but do not alter the ROS word data check.

Selector Channel Data Check

Invalid 1410 Characters

During selector channel read operations, invalid 1410 characters on the bus in to the translator cause a 1410 data check condition. The 1410 data check sets the wrong length record latch and turns on bit 1 (WLR) in the 2040 selector channel status byte.

Channel Data Check

Input data from the translators to the W registers is parity checked. Incorrect parity causes a bus-in parity error which sets the channel data check bit in the CSW.

1410 Data Check During File Operations

Selector channel overrun conditions may result if chained commands occur simultaneously on both file and tape. The emulator program error routine increments a counter at hex location EC44 and retries the file operation each time an overrun occurs. If the overrun condition fails to clear after 10 retries, the emulator routine turns on the 1410 data check bit in the 1410 channel status byte (GPR 13, byte 2 or 3, bit 5) and prints out an error message. When answering a service call for 1410 data checks, the customer engineer should determine first if a file operation is involved; if such is the case, he should check the contents of the counter at EC44 to eliminate the overrun condition.

Diagnostic Programs

The following diagnostic programs can be used to test and maintain the 1410/7010 compatibility feature:

System/360 Diagnostics

IDENTIFICATION	LOADER	PART NO.	DESCRIPTION
4F10	DM	5396212	Hardware Test 1
4F20	DM	5396215	Hardware Test 2
4F30	DM	5396218	Hardware Test 3

1410/7010 Diagnostics

Load the emulator program number 360 C-EU-728 followed by the individual 1410 diagnostic program. No other 1410 diagnostics should be run except the following:

IDENTIFICATION	DESCRIPTION
CS43C	Storage reliability
CS46B	Storage reliability
CU01	CPU reliability
CU06	Super scramble
C021	CPU error detection
RP01	1402 card reader/punch
ST02	System test

IDENTIFICATION	DESCRIPTION
T021	Multichannel interchange
T022	Tape record gap
WT01	1415 console I/O printer
W001	1403 printer
W002	1403 forms control

Additional information on the 1410 compatibility feature is found in *IBM System/360 Model 40, 1410/7010 Compatibility Feature, Field Engineering Theory of Operation,* Form Z22-2898.

Aids in Programming

When writing small programs for trouble shooting, the addition of a few instructions can save time and program steps.

Exclusive OR Instruction for SIO Routine

If you must write a diagnostic routine which has to alternate addresses or instructions; e.g., in I/O operations such as read-write and seek alternate addresses, an easy method is looping a small routine and changing one controlling factor, as in the I/O operations (CCW). This can be done with an exclusive OR instruction.

To alternate between read-write backward operations, use the same routine, but alternate between two CCW's.

```
I/C
ABC  –                          First instruction of the routine
....  –                         routing.
....  –                         Last instruction in the routine
        97  08  0  04B          modifies the command address
                                in the CAW with the exclusive
                                OR instruction.
        47  F0  0  ABC          Branch back to the start of the
                                routine.
```

4B (the last byte of CAW) contains lower part of the address of the current CCW. Assume this is 20 hex.

20 Hex = 0010 0000 in binary

08 = 0000 1000 is the modification factor of the exclusive OR instruction.

In the first exclusive OR operation, the contents of MS location 4B are altered from 20 hex to 28 hex. The next time it is changed back to 20, then to 28 and so on, as follows:

```
20 hex = 0010 0000
08 hex = 0000 1000  =  28
         0010 1000     at the end of first exclusive OR
                       operation
28 hex = 0010 1000
         0000 1000
         0010 0000  =  20 at the end of second exclusive
                       OR operation
```

This instruction can be used to program the machine into either of two separate loops using one basic routine flow, taking each loop alternately for every pass of the basic routine.

Supervisory Call (Monitor Call) Instruction

This can be used as a simplified load PSW instruction in a simple program; the PSW is obtained from the supervisory call new PSW in location 60 (hex) of main storage.

Another simple load PSW operation can be obtained by causing a program interrupt deliberately using an invalid instruction (for example, MULT DECIMAL in which L1 = L2). The new PSW is the program's new PSW.

Looping of Small Routines

If the machine check new PSW directs the machine operation back to the start of the program, the loop on ROS or check restart features can be used to full advantage as well as the normal log out operation.

Examples of Programming Aids

Assume a tape unit must write data and check the sense bytes, and that this program is to be looped.

Load the program into a master area as follows:

HEX MS LOCATION	HEX DATA				DESCRIPTION
448	0000	0210			Channel address word
44C-457					Not used
458	0100	0000	0A00	0500	"External new PSW" – enabled for external interrupts and interrupt key, given code letter A
460	4106	0000	0B00	0200	"SVC new PSW" – enables external interrupts and SC1 interrupts, given code letter B
468	0100	0000	0C00	0500	"Program new PSW" – given code letter C
470	0104	0000	0D00	0200	"Machine check new PSW" – given code letter D
478	0104	0000	0E00	0200	I/O new PSW – given code letter E
400	9C00	0180			Start I/O to required unit (unit 80 on channel 1)
404	9708	004B			Exclusive OR for next CCW
408	0A00				Supervisory call
410	0400	0080	0000	0006	CCW to place sense bytes into location 80
418	0100	0200	2000	0020	CCW calling a write (SILI flag)
500	D240	0048	0448		Move "master" CAW's from 448 to 048
506	D220	0200	0400		Move "master program" from 400 to 200
50C	47F0	0200			Unconditional branch to location 200

If the current PSW is similar to either the external or the program new PSW and the program set is running, the three program steps in locations 500, 506, and 50C are executed. These instructions load the data just entered (which can be regarded as the master area) into an execution area. Thus, the new PSW's entered into locations 448-480 are loaded into locations 048-080 (the PSW area) and the program keyed in is relocated into area 200 upwards so the master is not overwritten. The third instruction is used to branch into the start of the program. In location 200 (relocated from 400) a start I/O is issued to the required unit. The ma-

chine goes to the CAW in location 48 (448) and finds the CCW address is 0210. This CCW requires a sense operation. While this is happening, the processor continues with the exclusive OR instruction in location 204 (404). This particular type of exclusive OR will use the byte of data from the effective address (here, 04B, the last byte of the CAW, which is a byte of data; hex 10) and exclusive OR it with the I2 field of the instruction (08). The result of the exclusive OR is stored at the effective address (048) and is shown:

```
I2 field byte = 0000 1000
Data byte     = 0001 0000
Result        = 0001 1000
```

The next instruction is 208 (408). It is an SVC instruction and will load the SVC new PSW from location 060 (460). The PSW has the wait bit on and is enabled for SCI interrupts and the interrupt key. It accepts the end interrupts from the device started earlier with the start I/O instruction. The CAW is examined again and now has been altered by the exclusive OR instruction so that it points to a CCW at location 218 (418) (here, the write CCW).

The exclusive OR instruction has different data this time.

```
The I2 byte is still                = 0000 1000
but the data byte has changed to    = 0001 1000
the result is now                   = 0001 0000
```

It has changed back to the original value so that the CAW will point to the sense CCW again the next time through the loop.

If a machine check occurs when the program is looping or a loop on ROS/check restart occurs, the machine check new PSW restarts the program at the first instruction in location 200 (400).

Sense Command

Sense command is useful in fault-finding techniques because:

1. No mechanical movement of the I/O device is initiated.
2. Channel end and device end are returned at the same time, causing only one interrupt.
3. Using multiplex or selector channel, it is possible to single-cycle the complete operation, including data transfer and status handling.
4. Sense command does not reset the sense data in the I/O device.
5. Cycling is possible with a simple routine that can be entered from the console.
6. Progressive, small alterations to the instruction make it possible to check a wide area of the channel.

SIO Routine Using Sense Command

HEX MS LOCATION	IC IN HEX				DESCRIPTION
0048	0000	0400			CAW
0060	F006	0001	0000	0200	SVC new PSW
0070	F004	0002	0000	0200	Machine check new PSW
0078	F004	0004	0000	0200	I/O new PSW
	F004	0008	0000	0200	Current PSW in LS
0200	9C00	0XYY			SIO to device YY on channel X
0204	0A00				SVC, wait for interrupt
0400	0400	0080	0000	000N	CCW-Sense: N is equal to the number of sense bytes for the particular device.

The preceding routine may be modified easily to check command chaining and transfer in channel as follows:

0400	0400	0080	4000	000N	CCW-Sense with CC
0408	0800	0400	0000	0000	CCW-TIC back to previous CCW

Once the sense command has been tested, this routine may be further varied for read or write operations, and so on.

When using read or write commands in a device, use care in writing small loops to take into account possible interrupts. For instance, except to the control command, the TAU returns channel end and device end at the same time. This does not happen when issuing read or write commands to the IBM 1442 Card Read Punch.

I/O Scoping and Single-Cycling on Mpx Channel

Some multiplex devices can be single-cycled in data transfer routines. The IBM 1052 can read or write one data byte at a time; the IBM 1442 can punch (but not read) one column, and the IBM 1443 can store one byte in its buffer. To single-cycle a multiplex device, turn the rate switch to SINGLE CYCLE and use the single-cycle routine.

To scope multiplex I/O units, use diagnostic test F060S, an I/O scoping routine. If you have trouble loading F060S, set the rate switch to PROCESS, turn the CPU check switch to CHECK RESTART, and perform the following single-cycle routine: (Part numbers of F060S data, listing, and write-up are in System/360 General Service Aid No. 4.)

HEX MS LOCATION	IC IN HEX				DESCRIPTION
0048	0000	0400			
0060	8006	0001	0000	0000	SVC new PSW
0070	8004	0002	0000	0200	Machine check new PSW
0078	8004	0004	0000	0206	I/O new PSW
	0004	0008	0000	0200	Current PSW in LS
0200	9C00	00YY			SIO to device YY
0204	0A00				Enter wait loop till the channel end interrupt is taken.

HEX MS LOCATION	IC IN HEX				DESCRIPTION
0206	9D00	00YY			Clear the device end interrupt with a TIO.
020A	4780	0200			Branch back to SIO: if CC = 0.
020E	47F0	0206			Branch back to test I/O.
0400	XX00	0800	0000	00NN	CCW, where XX is the appropriate command and modifier bits while NN is the number of bytes transferred.

In the preceding routine, the initial-selection sequence may be repeated many times in the test I/O instruction. Thus, if you must scope it during the SIO instruction, use the sync provided from the AND of ROS address compare and MS address compare (01A-D3-J6D10 on KH142).

Using the IPL-Routine

The IPL routine generates an initial CCW of 0200 0000 60XX 0018 in main storage locations 0000 to 0007. Altering this CCW provides a quick and easy method of entering small routines for situations where single cycling is required. It is necessary only to set up the unit address in the load unit switches, ROS stop on 554 (QC121) and press the load pushbutton.

The initial CCW can now be altered manually to the required command code, data address, flags, and count. The system continues in the IPL routine, but operations are determined by the manually altered CCW. Therefore, it is possible to stop ROS at any selected point in the routine, and to single cycle through the suspect area.

This principle is applicable to M or selector channel and to most devices. For instance, it is possible to single-cycle through the complete write routine on the IBM 1052 or do a data transfer on a selector channel by using a sense command.

Check Restart on IPL

IPL can be used both as a quick check on channel operation or as a powerful tool for channel fault-finding.

As a first step a quick check can be carried out to determine whether the device or the channel is at fault. Do this by accessing different I/O devices by IPL.

If the fault is in the channel and if error checks are brought on before the end of the IPL routine, check restart causes a CPU check-out system reset and restarts the IPL routine. Thus, it is possible to scope almost the complete start I/O operation, as well as the data transfer. The optimum oscilloscope sync point is easily selected by setting up the sync on ROS compare, and the microprogram address on data keys.

IPL also provides a quick means of checking the I/O device by checking the data read into the main storage locations 0000-0023. Refer to "Check Restart."

Interrupt Key in Program Branching

The interrupt key could be used to start another program in case of any unexpected occurrences. For instance, if the program appeared to take an incorrect branch and overwrite part of itself, pressing the interrupt key could start another program which would load the damaged program area from a master area and restart from the first instruction.

Identification of Unexpected Interrupts

Unexpected interrupts can be traced on simple programs by placing a different code number in bits 36-39 of each new PSW. Then, a check on these bits in the current PSW shows the PSW that has been loaded because of the unexpected interrupt.

Program Restart (Hardstop Error Condition or Looping)

The programmer should foresee the possibility of a machine check condition and should provide for it in his machine check new PSW (location 70 hex in MS). It should be possible to restart many programs by manually loading this machine check new PSW into the local storage PSW, system resetting and starting again without reloading the program. (The customer should make full provision for this failure although the customer engineer should remember this point. Normally, the customer engineer is not expected to restart the customer's program.)

General Diagnostic Hints

IBM System/360 Model 40 Installation Manual, Form Y22-9500 gives full information on cable layout, terminations, and pin-allocation diagrams of the interface serpent connectors.

Device End

Device end, alone, can be accepted only at machine-language program level. When device end is presented at microprogram level, it is rejected, but the number of the I/O unit that presented device end is retained. The unit is selected later when the program accepts the interrupt.

IBM 1442 Card Reader-Punch

The IBM 1442 idling control is inoperative (the motor continues to run) until both channel-end and device-end interrupts are accepted by the channel.

Program language/one (PL/I) card code decodes a blank as hex 40, which means that blank cards can be

used in the IBM 1442 for various IPL tests. Data transferred into main storage locations 0000-0023 is hex 40 in every byte.

Instruction Counter Display

Displaying the instruction counter of the PSW (IC position of the storage select switch) causes the address lights to show the IC value and the main storage data lights to show bits 32-47 of the PSW. (Bits 34 and 35, the condition code, are displayed in bits 2 and 3 of byte 0.) Instruction stepping and displaying IC allows execution of one instruction to check on the resulting condition code. This technique is especially useful in small I/O loops. (See "Small I/O Loops-Instruction Stepping.")

Interrupt Buffer

The interrupt buffer (LS2A) checks pending mpx interrupts only if the mpx interrupt request latch is set. Normally, the interrupt buffer does not contain the unit number of the device being serviced.

Power On-Off

Power may be turned off any unit in a line of I/O devices except the last one in line; this action removes voltage from the terminating resistors and allows the interface lines to float.

Single-Cycling

When single-cycling through an operation, note that a one- or two-cycle delay may occur between the time the tag line comes up and the time data appears in the IF register display.

The IBM 1442 can be single-cycled through a write data service.

The IBM 1052 can be single-cycled through a read or write command.

Data may be entered from the keyboard when the proceed light comes on.

Small I/O Loops-Instruction Stepping

Entry to the manual stop loop is always preceded by the display microprogram. The manual stop loop can be used if a particular status is expected in the CSW. Set the main storage address keys to hex 0044 (CSW status byte), the storage select switch on MS, and the address compare switch on Stop on MS. Pressing START causes the CPU to stop each time the CSW is accessed in main storage; the data lights display the status byte. When the expected status is obtained, look up the I/O old PSW for the unit that presented the status.

Displaying main storage location hex 44 while instruction stepping through small I/O loops permits observation of channel status as it is stored because of interrupts or test I/O operations. Channel-end and device-end sequencing and associated unit exception or unit check can be observed.

System Reset

System reset clears both the multiplexor and selector channel UCW areas.

Miscellaneous Hints

Microprogram instruction LAS loads the channel and unit numbers from the load switches into R0 bits 4-7 and R1 bits 0-7. R0 bits 0-3 are determined by the setting of the storage select switch.

A write command results in a WLR indication unless it is suppressed by the SILI flag. This hint applies only to variable-length devices e.g., tape units. The I/O old PSW gives the unit number of the device last serviced at machine-language program level.

Diagnostics

There are several distinct diagnostic monitor programs which satisfy the various environmental conditions which may occur with the System/360 Model 40. These DM's provide these functions:

1. Control of program loading
2. Control of diagnostic program execution
3. Interruption handling
4. Customer engineer options (halt, loop, bypass, etc.)
5. Interface with the operating system
6. Standard error messages
7. Diagnostic communication with the customer engineer

The following chart shows the DM's provided for the System/360 Model 40 and their characteristics:

CHARACTERISTICS	DM1	DMA8	DMK
Number of bytes	3K	8K	4K
Load via IPL	x	x	x
Single System	x	x	x
Load from cards	x	x	x
Load from tape	x	x	x
Sequential execute		x	x
Customer engineer			
Printer		x	x
Typewriter		x	x
System console panel	x	x	x

For further details of maintenance program packaging, see the appropriate documentation with the diagnostics, or the program logic manual with the diagnostic monitors. For general operating procedures, refer to the *System/360 Diagnostic Program User's Guide*, Part 5396096.

Log Out Retrieval Programs

System Environment Recording (SER)

SER comes into play as a result of certain checks (both CPU and I/O) when Operating System/360 is being used. The program package is designed to collect and edit system status information and specified auxiliary data (time, I/O activity status, program ID, etc.). This information (the environment record) is transferred to a designated area on the OS/360 system residence device for storage.

For further details on SER programs, see Operating System/360 publications *Storage Estimates*, Form C28-6551 and *Operator's Guide*, Form C28-6540; Operating System Program Logic Manual *Fixed Task Supervisor*, Form Y28-6612.*

Environment Record Edit and Print (EREP)

This program provides for the retrieval and print out of environmental records. The program permits easy usage, extraction, and organization of environmental records according to specified CE options.

For further details on EREP programs see Operating System/360 publication *Utilities*, Form C28-6586 and Operating System Program Logic Manual *Utilities*, Form Y28-6614.*

Systems Environment Record Edit and Print (SEREP)

This program is a stand-alone program providing for retrieval of environmental records after a machine check or I/O permanent error for a print out.

Figure 9 provides a list of the availability of these programs per configuration or unit.

Configuration or Unit	SEREP	SER	EREP	Bring Up	Functional Test	Circuit Test	Check Circuit Test	DMI	DMA 8	DMK
Multi System									X	
Single System									X	X
2040 CPU	X	X	X	X	X	X	X	X	X	X
Main Storage				X	X	X				
Storage Protect					X	X				
Bump Storage					X					
ROS					X		X			
Local Store					X		X			
MPX Channel	X	X	X		X		X			
Channel to Channel					X					
Direct Control					X					
Shared Storage					X					
1052 Adapter					X					
Selector Channel	X	X	X		X		X			

Figure 9. Programs Available for System/360 Model 40

For more information on the SEREP program, see the appropriate program description or refer to IBM Sales and Systems Guide, *System/360 General Programming Considerations*, Form Z20-0005.*

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Console

- **Eight main sections contain indicators, rotary switches, pushbuttons, keys and toggle switches.**
- **Customer uses panel H to run programs.**
- **Customer and customer engineer use console panel G to debug programs.**
- **Customer engineer uses console panels A, C, D, F, and G to debug system.**
- **Customer engineer uses console panel C to run built-in diagnostics.**

The console of the IBM 2040 (Figures 13, 14, 15, and 16) divided into eight main console panels labeled A to H for reference. Each console panel groups switches and indicators according to the function they perform.

The types of switches used on the console are:

1. Rotary and roller switches, defined position by position.
2. Pushbuttons, active when depressed.
3. Keys, active in the down position.
4. Toggle switches, active as defined by console panel engraving.

In general the console performs four specific functions.

Running Tested Programs: The only pushbuttons and rotary switches used by the customer are in console panel H. No other manual controls are needed by the customer to run his jobs. The operator puts the system in or out of working condition by pressing the power-on or power-off pushbuttons. He can load his program by setting, in the load unit rotary switches, the channel and device number from which he wants to load his program and then pressing the load pushbutton. All other program controls are defined by the program itself. The interrupt pushbutton is the only way an externally initiated program change can be made by the operator.

Debugging Programs: Console panels G and F are used. Console panel G gives access to system areas accessible by the program (fixed or floating point registers, main storage, storage protect, PSW in local storage). These areas control instruction step or stopping the system at predetermined storage addresses. The initiation of log out in case of a machine error can be modified to error stop. Start display, and store are only active if the system is in the stop loop (T clock running).

Debugging Machine: The console panels previously described can be used, but additional console panels D and part of C give access to most parts of the system accessible by microprogram. Console panel C contains the channel selection switches and interface debugging facilities. To store or display registers used by the microprogram, the system must be in hardstop (T clock stopped).

Running Built-in Diagnostics: Console panel C contains the rotary switch to select a particular internal diagnostic.

Console Panel A

Check Indicators

- **Indicators are arranged on the console in the order of an error sequence.**

There are three major error check latches on the system.

They are:

1. Control check latch
2. Early check latch
3. Late check latch

Assuming that all three error latches are on, the most significant error latch is the control check latch. This is because some internal error forces the control check latch on. This internal error has caused other error conditions which have turned on the early and late check latches. The check indicator panel has been arranged to isolate the source of the failure.

There is a definite order of occurrence in the three major check latches. In addition, there is an order of occurrence in the error conditions that force the major check latches on. The major error check latches are useful with intermittent failures. An intermittent error condition could occur and pass, but either the control, early, or late check latches would have been set. This forces the machine to a hardstop, or a log out of the conditions at failure. As a result of this the error conditions that caused the failure may not be indicated, but either the control, early, or late check indicator will be on. The most significant error condition can be found by scanning left to right and top to bottom on the indicator panel (Figure 14).

Therm (Thermal Indicator)

This indicator indicates a particular section of the system is over-temperature; it is the OR of individual thermal checks. The internal CE panel thermals indicate individual failing sections (Figures 11 and 12).

NOTE: The following indicators are not present on the revised Mid-Pac power supply released with **EC255055.**

PWR = Power Supply Unit
MS = Main Storage
ROS = Read Only Storage
GA = Logic Gate A of Frame 01
GB = Logic Gate B of Frame 01

The indicator remains illuminated until the thermal reset procedure is performed or power is turned off and then turned on.

O/L (Overload)

This indicator shows an over-current condition exists in the associated module. Each module of the power supply has an indicator mounted on an SMS card.

Detection of an over-voltage results in an over-current indication of the relevant supply.

The mid-pac power supply has a circuit breaker on each power supply module in the power supply section; this CB trips with an over-current condition. The reset for over-current on the high frequency power supply is located on the converter/inverter module. The over-voltage reset is located in the upper front section of the power supply unit.

ROS ADR (Read Only Storage Address Bus Parity Check)

This indicator indicates an internal ROS addressing failure. It also checks for equal comparison of CF field bit with the parity bit of ROSAB.

ROSAB may contain ROAR or either of the two ROSCAR's of selector channel.

The address check forces a control check.

NOTE: The next ROS address in ROAR cannot be relied upon to be correct.

ROS DATA (Read Only Storage Data Parity Check)

This indicator shows a parity error (even parity) has been detected in the current ROS control word.

ROS data check forces a control check, and the address of error is retained in ROBAR.

The ROS control word in error can be seen on the internal CE panel.

NOTE: The next ROS address in ROAR cannot be relied upon to be correct, because bit pick-up or bit drop-out could have occurred in the section of the control word which contains the next ROS address.

D/Y8 (Diagnose and not Y8)

This indicator indicates an undump has occurred with Y8 off, and it forces a control check.

Y8 prevents further dumps during a dump/undump sequence.

D/Y8 will be turned on any time an undump is executed with Y8 off. The diagnose instruction can be used to force the D/Y8 error by causing a dump and undump with stat Y8 off (a log out will result from the program forced error).

CTL (Control Check)

This indicator shows a ROS decode failure, (ROS ADR, ROS DATA, D/Y8) or that a LOG microprogram command has been issued.

Control field indicators on the CE panel isolate decoder checks to the particular control field.

ROBAR contains the failing address.

Control check inhibits changing the ROS sense latches, setting ROBAR, and changing of the ALU control register.

Control check may force a late check. If the control check is enabled, it stops the T clock at the end of the present cycle.

Control check starts a log out if enabled (Y12 off, and Y15 off). Y12 is on during internal ROS diagnostics, and microprogram log out. Y15 is on during IPL when hardstop is forced if it is enabled.

NOTE: (1) The next ROS address contained in ROAR cannot be relied on as correct. This is because a decoder failure could have occurred in the CB or CC fields. (2) Any odd number of active decoder outputs will not result in a control check. (3) Only control checks are active during log out.

LS Read (Local Storage Read)

This indicator shows a parity check of local storage output data in the R register, and it is checked at P4 time.

Local storage read is checked in every cycle including hardware cycles.

The early check latch is set on the next cycle.

NOTE: (1) R register and LSAR failure contents are lost as a hardstop does not occur until the next cycle. Reference to the CAS sheets, however, allows this information to be recovered. (2) Because of close timing conditions the last microinstruction prior to a dump is not local store read checked.

MS ADR (Main Storage Address)

The MS ADR check is a parity check of the storage address bus (SAB) (from A or S register). It forces an early check.

MS DATA D0 (Byte Zero of D Register)

This indicates a D0 parity check has occurred on recognition of even parity. It forces an early check.

MS DATA D1 (Byte One of D Register)

This indicates a D1 parity check has occurred on the recognition of even parity. It forces an early check.

NOTE: Good parity is forced into main storage even if parity in D register is bad.

R REG (R Register)

RX (Extension of R Register)
R0 (Byte Zero of R Register)
R1 (Byte One of R Register)

Each indicates that a parity check has occurred, and forces an early check.

NOTE: Early check will not occur if the error is detected during log out.

MS Protect (Main Storage Protect)

The CPU and channel key registers are checked for odd parity on the CPU-channel tag (key) bus.

The storage protect data register is checked for odd parity on the compare bus. MS protect forces an early check.

State (Staticizers)

The four YA stats and the four YB stats are checked for odd parity. Stats forces an early check.

ALU (Arithmetic Logic Unit)

EX (Extended ALU Input, EX Register) indicates an ALU EX register parity error has occurred. It also forces an early check.

P Register Parity: The P latches are checked for odd parity, and it forces an early check.

Q Latches Parity: The Q latches are checked for odd parity, and an early check is forced.

NOTE: The Q bus is not parity-checked when set from external interrupt latches, channel interrupt latches, or direct data register.

Early (Early Checks)

This indicates that an error has occurred early in a machine cycle. It also indicates that one of these errors has occurred:

1. LS read
2. MS ADR parity check
3. MS DATA – D0, D1 parity check
4. RX R0, R1 parity check
5. Main storage protect – key, or data register parity check
6. Staticizer parity check
7. ALU – EX, P, Q

The early check latch is set at P1 del, T2 del, or P3.

Early check inhibits change of ROS sense latches, inhibits setting of ROBAR, and changing ALU control latches.

The T clock stops at the end of the cycle in which the early check latch (if enabled) is set. Early check starts a log out if enabled and Y12 and Y15 are off.

Hardstop is forced if it is enabled during internal ROS diagnostics and IPL routine.

LSAR (Local Storage Address Register Parity Check)

LSAR is checked for odd parity; LSAR forces a late check.

ALU Skew (Skew Select Parity Check)

The skew select latches are checked for odd parity. It forces a late check.

NOTE: The skew select latches are not checked when Q bus is set from external interrupt, channel interrupt or direct data register.

ALU Function (Arithmetic Logic Function Check, Decoder Check): indicates improper decoding of the ALU control register, and forces a late check.

2W (Two-Wire Check): A two-wire check for errors is made at the ALU binary output, the carry stats, and the extension bits (5, 6, 7). Each two-wire check is indicated separately, by bit position on the internal CE panel (Figures 10, 11, 12).

A two-wire check forces a late check.

NOTE: Each logical state in the ALU is represented by two lines that must always be of opposite polarity. These two lines have separate generating circuitry to make this method of checking accurate.

ROAR (Read Only Storage Address Register Transfer Check)

Information transferred to ROAR may come from any of these sources:

1. CD field
2. CA field
3. Q bus

When ROAR is set by any of these fields a comparison is made between the ROAR bits set by this field and the field itself. They must be both even or both odd. When the ROAR condition is set, it forces a late check.

NOTE: This indicator is referred to as a DAQX ROAR check. D for CD field, A for CA field, Q for Q bus, and X for transfer.

Channels

Any channel check is indicated, and forces a late check.

NOTE: Bus in panel check during a data service only shows as a channel data check in the status byte.

Mpx (Multiplex Channel): indicates that one of these errors has occurred:

1. Mpx IF tag check.
2. Mpx IF control check.
3. Mpx IF parity check.

Select Voltage Switch Position	Read on Meter Range	Used for	Adjusted from	Comments
-3v	Mid-Upper	Logic Supply	Pot on SMS Card in Power Supply	
+3v	Mid-Upper	Logic Supply	Pot on SMS Card in Power Supply	
+6v	Mid-Lower	Logic Supply	Pot on SMS Card in Power Supply	
-18v	Upper-Quarter	Logic Supply	Pot on SMS Card in Power Supply	
+24v	Upper-Quarter	Relays, Indicators, Contactors	Not Adjustable	
+48v	Mid-Lower	1052 Feature	Pot on SMS Card in Power Supply	
+6M	Mid-Upper	Margin Supply	6M Pot on Internal CE Panel	Adjusts from 4.4 to 7v to Marginal Check SLT Gates A and B
ROS	Mid-Lower	ROS Drive Current	ROS Drive Pot on Internal Panel	Adjusts from 60 to 73 ma, 66 ma Normal Setting
LS/Vm	Mid-Lower	Bias LS	LS/Vm Pot on Internal CE Panel	-6 to -9v Temperature Dependent Power Supply
LS/Vxy	Mid-Upper	X Y Drive for LS	LS/Vxy Pot on Internal CE Panel	Adjusts from +1.5 to +3.5v
SP/Vxy	Mid-Upper	Storage Protect Feature	SP/Vxy Pot on Internal CE Panel	Adjusts from +1.5 to +3.5v
MS/Vz	Mid-Lower	Main Storage Z Drive	MS/Vz Pot on Internal CE Panel	Adjusts from 52 to 64v at 4 amps Overvoltage Cut-Out Above 64v
MS/Vxy	Mid-Lower	Main Storage X Y Drive	MS/Vxy Pot on Internal CE Panel	Adjusts from 52 to 64v at lamp; Overvoltage Cut-Out Above 64v

Figure 10. High Frequency Internal CE Panel Controls

4. Mpx channel control check. The Mpx condition forces a late check.

SC1 (Selector Channel 1): indicates that one of these errors has occurred:

1. ROSAB parity check.
2. SAR parity check.
3. T register parity check (each byte is checked).
4. Storage protect key register (checked on storage protect key bus).
5. W0 parity check and interface bus-in parity check.
6. Flag register parity check (bits 0-3 only).
7. Channel data check.
8. Channel control check.
9. Interface control check. The SC1 condition forces a late check.

SC2 (Selector Channel 2): is the same as SC1.

Late (Late Check)

This indicates that an error has occurred late in a machine cycle.

It also indicates that one of these errors has occurred:

1. Two-wire check of the ALU output extension.
2. ROAR transfer check.
3. Skew select error.
4. LSAR parity check.
5. ALU function check.
6. ALU two-wire check.
7. Channel checks (Mpx, SC1, SC2).

The late check latch is set at T3 or P3 del for all error conditions.

It inhibits ALU control changes, and the setting of ROBAR.

It stops T clock (if enabled) at the end of current

machine cycle, and starts log out (if enabled) and Y12 and Y15 are off.

Hardstop is forced if it is enabled during internal ROS diagnostics and IPL routine.

μP (Microprogram Stop)

This indicates a microprogram stop has been executed. It is used in internal ROS diagnostics only, and is given by the control signal, STP CI in the CAS block.

ROBAR contains the address of the halt instruction. This indicator forces the machine into the hardstop state.

Conditions (for which this indicator is active) are machine errors under microprogram detection.

The indicator sets system reset latch if it is in check restart condition.

NOTE: Machine status charts (MSC) may be used to determine the failing instruction in some cases (MSC page FCZ. 00. 001). See microprogram check in this manual. (CPU and selector channel checkout.)

Machine Condition Indicators

H/STOP (Hardstop)

This indicates that the machine is in hardstop state, and that the T clock is stopped.

The machine enters into a hardstop state for:

1. Single cycle mode.
2. Microprogram stop.
3. Stop on ROS.
4. Stop on MS and ROS.
5. Error during CPU checkout, IPL, or internal diagnostics if enabled.
6. Error during log out.

Log (Log Out)

This indicates a hardstop during log out. Light cannot be seen during the log out operation.

Log out is initiated by any of the following:

1. Logic detection of a machine error.
2. Depression of the log out pushbutton.
3. Microprogram detection of a machine error.
4. The diagnose instruction, by forcing an error to occur.

DSAB (Disable)

This indicates that the machine is operating in disable mode. Operations continue regardless of error conditions recognized.

Error conditions are latched and cause operation of normal error routines when enabled.

DP1 (Dump 1)

This indicates a dump has been installed. It is driven by dump latch, and is initiated by multiplex channel for data service.

S to SAB (SC1/SC2)

This indicates which S register for selector channel operation is now being gated to the storage address bus.

Console Panel B

Emergency Pull

Operating the emergency pull knob causes immediate de-energizing of all power supplies in the system.

Normal power-off sequencing is eliminated with this switch. The switch contains a mechanical interlock and must be manually reset by the customer engineer before power can be restored to the system.

This switch does not remove power from mainline circuit breakers or I/O device main-power breaker inputs.

It is active in all modes.

For further details, see "Power Supply".

Console Panel C

Diagnostic Control Switch

This switch selects internal ROS diagnostics. If the system is enabled, errors force a hardstop state.

A diagnostic is started by pressing the start button (panel G), and can be stopped only by depressing system reset or log out (panel G).

If the switch is in any position other than the off position, the test indicator will light.

LS Pattern

Worst-case data bit patterns are written in each location of local storage on the first and third tests, the complements are written on the second and fourth tests (QS121). Patterns on first and second tests are then read and checked for parity errors as a test for sense and inhibit noise.

Third and fourth tests contain worst-case bit patterns that are performed essentially for checking the parity bit.

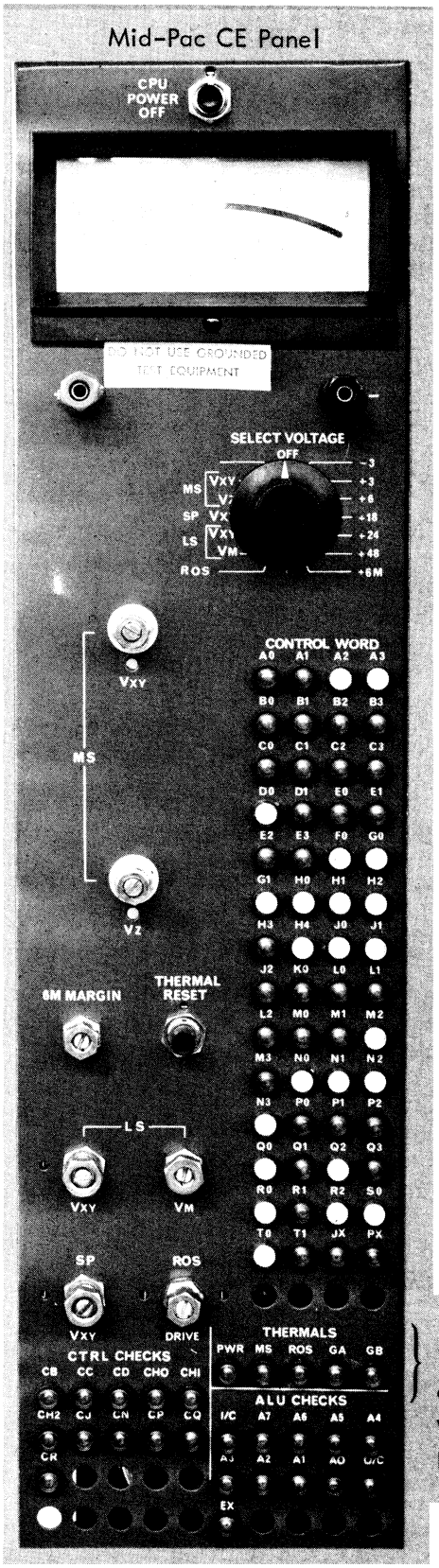
The failing address is available in LSAR; data in error is available in the A register.

LS Address

Its own address is written into every local-storage location (QS121); each location is read and checked. Data in error is available in the A register.

The failing address is available in LSAR.

Comparison of the A register and LSAR indicates the address bit in error.



These thermal indicators are not on machines with revised Mid-Pac power supply (EC255055).

Figure 11. Model 40 Internal Console Panel (Mid-Pac PS)

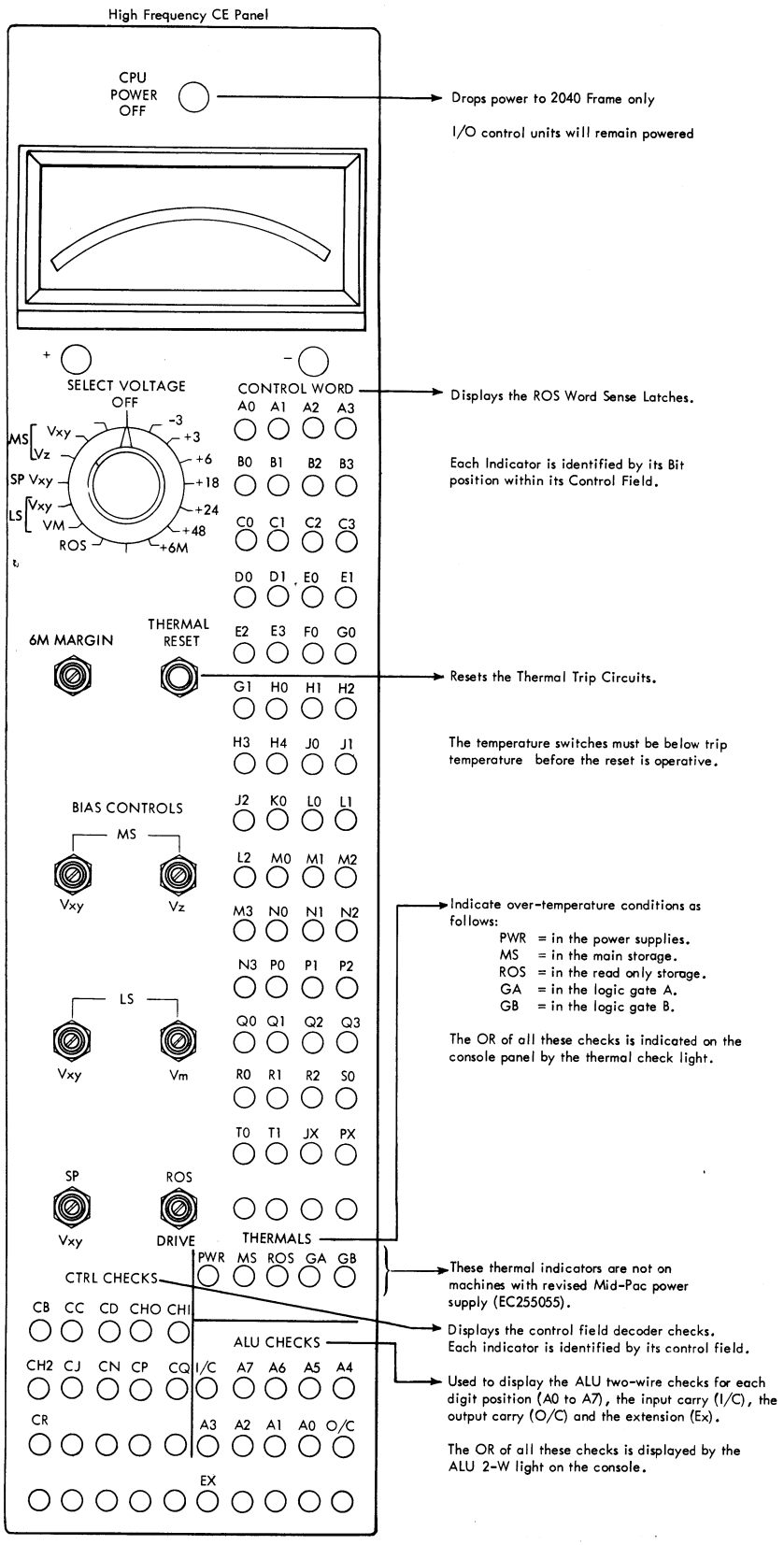


Figure 12. Model 40 Internal Console Panel (HF)

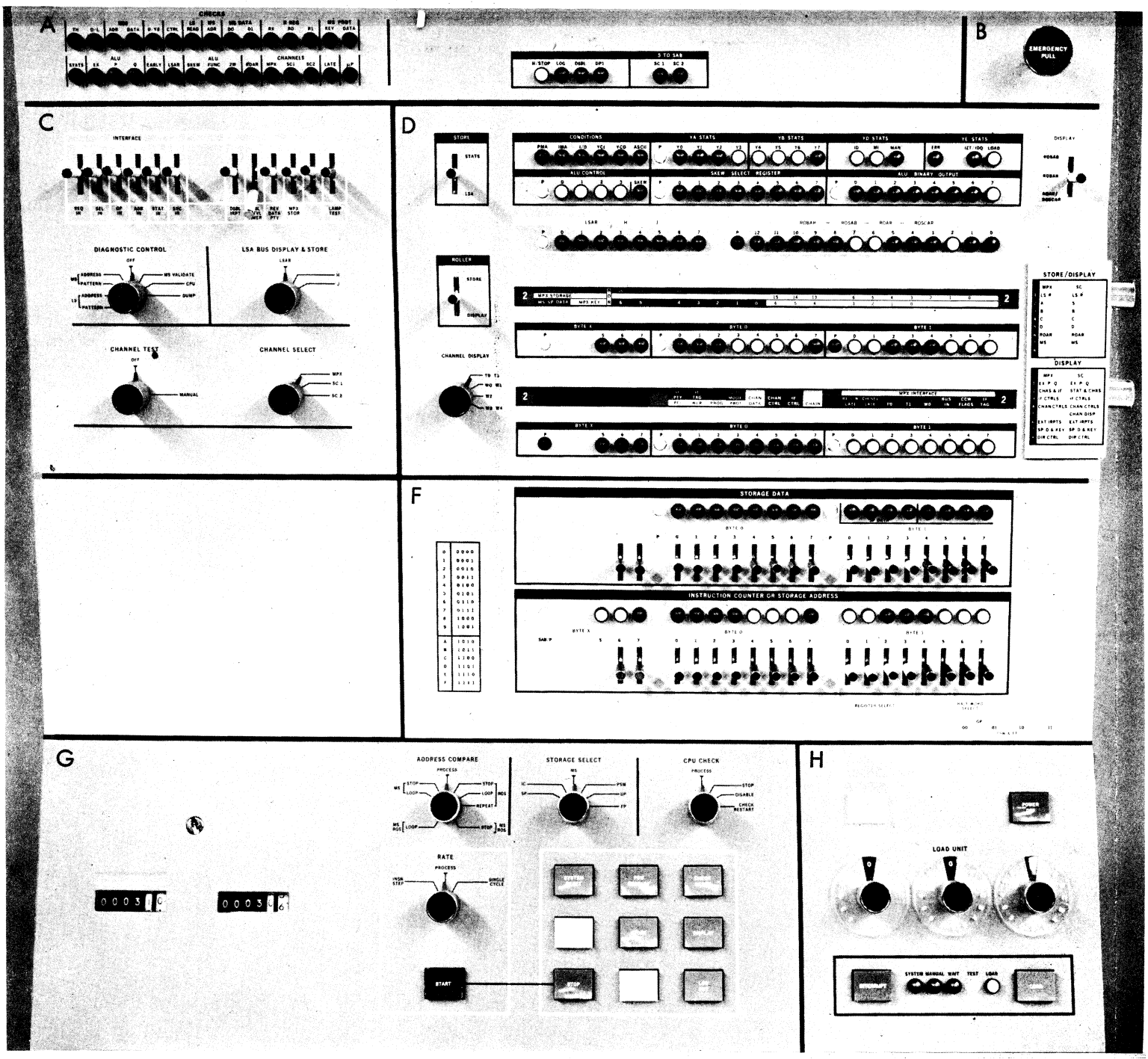


Figure 13. Console – IBM 2040 Processing Unit

		ROS				LS	MS	MS DATA		R REG			MS PROT	
THERM	O/L	ADR	DATA	D/Y8	CTRL	READ	ADR	D0	D1	RX	R0	R1	KEY	DATA
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)
		ALU					ALU			CHANNELS				
STATS	EX	P	Q	EARLY	LSAR	SKEW	FUNC	2W	ROAR	MPX	SC1	SC2	LATE	μP
(16)	(17)	(18)	(19)	(20)	(21)	(22)	(23)	(24)	(25)	(26)	(27)	(28)	(29)	(30)

This figure shows the order of significance when scanning for source error condition, starting at 1 through 15 then 16 to 30.

Figure 14. Check Indicators

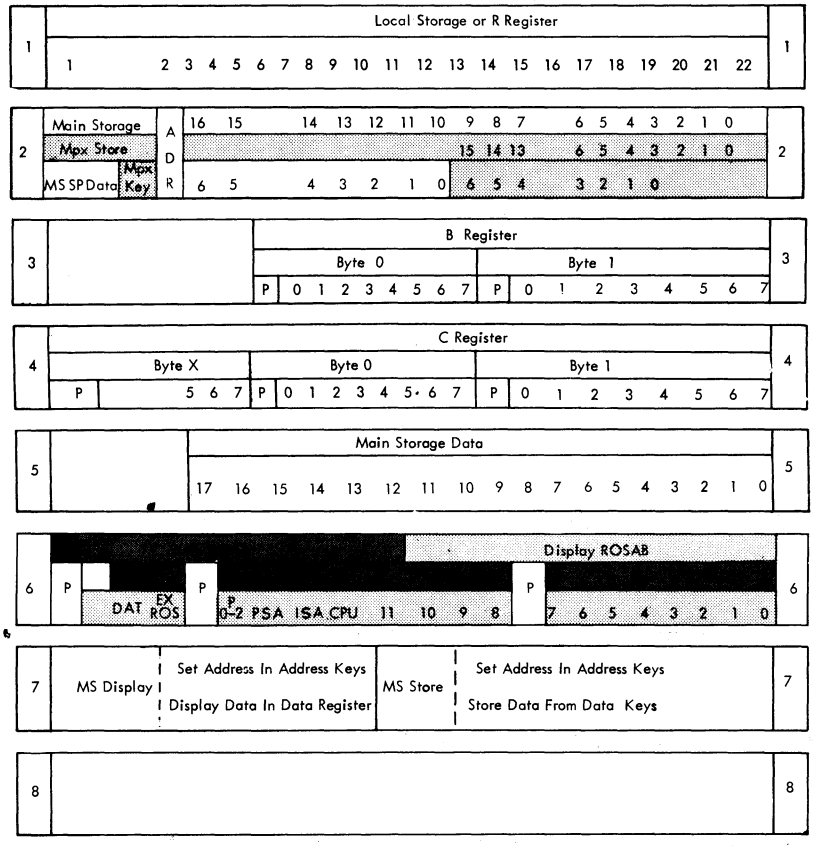


Figure 15. Roll Chart — Upper

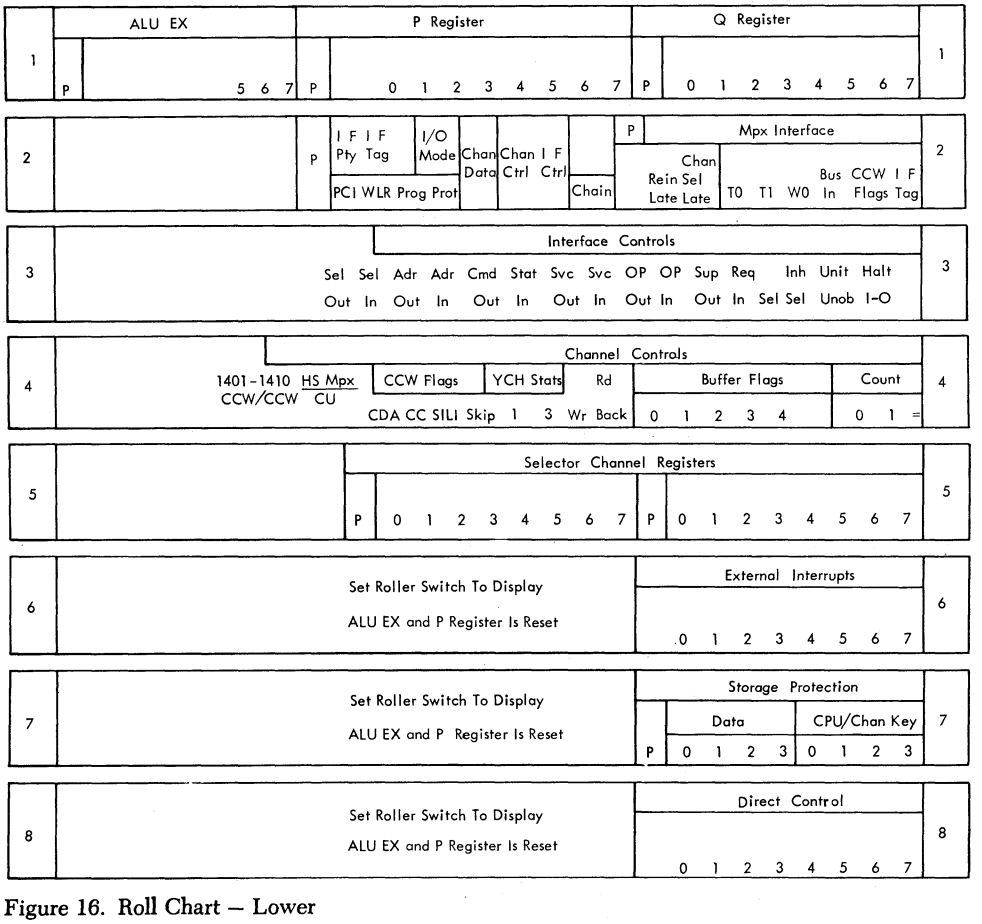


Figure 16. Roll Chart — Lower

MS Pattern

Worst-case data bit patterns are written in each location of main storage on the first and third tests, the complements on the second and fourth tests (QS191). Patterns on first and second tests are then read and checked for parity errors as a test for sense and inhibit noise.

Third and fourth tests contain worst-case bit patterns that are performed essentially for checking the parity bit.

The failing address is located in the A register, and the data word in error is contained in the D register.

MS Address

Byte 1 of its own address is written into every main-storage location (QS191); each location is read and checked.

Data in error is available in the D register.

The failing address is available in the A register.

Operation is duplicated with byte 0, and then byte X of the address of each main-storage location.

MS Validate

This reads out and rewrites the same word with correct parity in each location of MS (QS191).

The machine hardstops after the rewrite if a parity error is detected. An error address is contained in the A register while the D register contains the error word.

CPU

The CPU switch selects the CPU checkout microprogram in ROS (QS111).

This is used in conjunction with machine status charts when diagnosing system errors.

CPU checkout is extended to include the selector channel, when the selector channel feature is installed.

Dump

This diagnostic provides a means of looping the dump and undump routines.

Channel Test Switch

The channel test switch is used in conjunction with the channel select switch (panel C). This switch should be in the off position for formal processing.

Manual SEE P. 40

The manual position is used with the interface keys and single-cycle mode while cycling a channel microprogram.

Load unit switches are set on bus-in during single-cycling.

To single-cycle through a channel microprogram without using any I/O unit, the channel-test rotary switch is set to the manual position. The multiplexor channel is the only channel that may be single-cycled in manual mode.

Every time the microprogram brings up an out tag, the corresponding in-tag reply can be given using the six toggle switches in console (panel C). The information on bus-in is taken from the load unit switches.

Note that select-out is prevented from going out on the interface.

Channel Select Switch

The channel select switch selects a channel for display and test. It is used in conjunction with the channel test switch, and is effective in all modes.

It selects the channel for display of positions 2, 3, 4, 5, and 7 of the display roll switch (panel D).

Mpx Position

This position selects multiplex channel for display or display and manual test.

With the channel test switch off, the multiplex channel is selected for display. When the channel test switch is set to manual, the multiplex channel is selected for display and manual test.

SC1 Position

This position selects SC1 for display or manual test. With the channel test switch off, selector channel 1 is selected for display. When set to manual, selector channel 1 is selected for display and manual test.

SC2 Position

This operation is the same as the SC1 position, except that selector channel 2 is now being used.

LSA Bus Display and Store Switch

This switch displays or stores these registers:

1. Local storage address register
2. H register
3. J register

It is active only in the hardstop state.

Store/display action is controlled by the store toggle switch in panel D.

Address keys for byte 1 supply data to be stored in the selected register.

NOTE: (1) LSAR contents are invalid unless the switch is in the LSAR position when a hardstop is encountered. (2) Store or display of other than LSAR

destroys LSAR contents. An LSAR check is obtained when in a hardstop state and the LSA switch is returned from any other position to LSAR.

Manual Interface — Mask and Test Tag Keys

These keys are used with the manual position of channel test to simulate control unit signals. They are active in the down position.

Manual interface tag keys simulate their respective tags and are:

REQ IN	Request In
SEL IN	Select In
OP IN	Operational In
ADR IN	Address In
STAT IN	Status In
SVC IN	Service In

The interface sequence responses by the CPU on data service may be checked quickly with the manual interface keys in console panel C. Proceed as follows:

1. Set the channel select switch to the mpx position.
2. Set the channel test switch to the manual position.
3. Set the upper roller switch to display ROAR (position 6).
4. Set the lower roller switch to display the IF controls (position 3).
5. Set the load unit switches to 000 and press system reset.
6. Set the rate switch to single cycle and the address compare switch to stop on ROS.
7. Set the operational in and address in keys down.
8. Set ROS address 668 hex (QA011) in the storage data keys.
9. Set the rate switch to process and press start. When the machine stops, ROAR should display 668 hex and these interface lamps should be on: address in, command out, operational out, and operational in.
10. Restore the address in key and reset the storage data keys to ROS address 6FD hex (QA011).
11. Depress start. When the machine stops, ROAR should display 6FD hex and these interface lamps should be on: operational out and operational in.
12. Reset the data key to ROS address 657 hex (QA091).
13. Set the service in key on and depress start. When the machine stops, ROAR should display 657 hex, and these interface lamps should be on: service in, operational out and operational in.
14. Reset the data keys to ROS address 676 hex (QA091) and depress start. When the machine stops, ROAR should display 676 hex, and these interface lamps should be on: service out, service in, operational out, and operational in.
15. Reset the data keys to ROS address 65B hex.
16. Restore the service in, and then the operational in keys and press start. When the machine stops, ROAR should display 65B hex, and the operational out interface lamp should be on.

Miscellaneous Toggle Switches

DSAB IRPT (Disable Interrupt)

This prevents the channel operation from interrupting CPU while a CPU operation is being tested. It also inhibits microprogram interrupts causing a dump.

This key is effective in all modes, and is active in the down position.

Dumps are inhibited without setting the inhibit dump stat (Y8).

This key also prevents automatic setting of ROAR for dump microprogram routine.

DSAB INTVL Timer (Disable Interval Timer)

This is used to prevent the timer from interfering with system operation.

This key is effective in all modes and is active in the down position.

It resets the four-bit counter, and the non-zero latch to zero state.

NOTE: If a customer's program is likely to exceed the time allowance for completion, disabling the timer allows the program to continue to completion.

REV Data (Reverse Data Parity)

This provides a means of entering even-parity bytes of data from the console data keys to the D register. Data may be entered in either a hardstop state or in the manual stop loop.

NOTE: The D register output to main storage is in correct parity regardless of the operation of this key. Parity generation on the output of D register assures odd parity.

Mpx STORE (Multiplex Storage)

This is used to store and display multiplex storage. It may be used to display or store unit control words.

This key is effective in all modes, and it allows manual addressing of multiplex storage, regardless of the status of the (Mpx) stat (Y1).

NOTE: The Mpx store key is effective in all modes. It should not be active during normal processing as the system obtains access to multiplex storage when it is requesting main storage information.

Lamp Test

This test is active in all modes, and active in the down position, and lights all indicators except test light.

Console Panel D

Conditions Indicators

PSA (Protect Storage Address)

This indicates that an invalid key has been sensed.

This indicator is driven directly from the protect storage address latch. When the contents of the storage protect register do not match the contents of the CPU/channel key registers and the key register is not zero, a PSA condition exists. This programming error, when detected by the microprogram, stops the normal sequencing of the program and stores the current PSW (byte locations 28-2F). A new PSW (byte locations 68-6F) is loaded which initiates the program check subroutine. This routine attempts to rectify the cause of the interrupt.

ISA Indicator (Invalid Storage Address)

This indicator shows that the capacity of main storage or multiplex storage has been exceeded.

ISA occurs when an address specifies any part of data, an instruction, or a control word outside the available main storage area for the particular size system. This programming error is detected by the microprogram and stops normal sequencing. It stores the current PSW (byte locations 28-2F) and loads a new PSW (byte locations 68-6F), which initiates the program check subroutine. This routine analyzes the condition and attempts to rectify the cause of the interrupt.

I/O (Input or Output State)

This indicates the CPU latch is off (a selector channel operation). The CPU latch is reset by a microprogram.

An I/O state is forced during selector channel operation by blocking the output of the CPU latch.

An I/O state causes a different translation of ROS B and C fields.

NOTE: Do not confuse this with reinterrupt.

YCI (Indirect Carry Stat)

This indicates the on/off state of the indirect carry stat, and a carry out on an indirect ALU function.

YCD (Direct Carry Stat)

This indicates the on/off state of the direct carry stat, and also indicates a carry out on a direct ALU function.

ASCII (American Standard Code for Information Interchange)

This indicates the system is in the ASCII mode. It is a result of the ASCII (bit 12) in the PSW having been set to a binary one.

YA Stats

These stats indicate various system conditions used to control machine functions.

They can be set or reset from:

1. Four-bit emit field in microinstruction.
2. ALU output under microprogram control.
3. Console data keys or system reset operation.

They can be sent along with the YB stats to the Q latches under microprogram control.

Parity Stat of YA Stats

This indicates the status of the parity stat for the YA and YB stats.

Odd parity must be maintained for the YA and YB stats.

Y0 (Storage Stat)

This indicates the on/off condition of the Y0 stat.

When on, it allows protect storage address (PSA) to force the SAT condition.

Y1 (Y1 Stat, Multiplex Storage)

This indicates on/off condition of the Y1 stat, and allows access of multiplex storage for multiplex channel operations.

It also allows access to protect tags for multiplex channel.

Y2 (Y2 Stat, Multi-purpose)

This indicates on/off condition of the Y2 stat, and is used for multi-purpose control.

The Y2 stat performs several functions:

1. It is used with Y3 for condition code (set up PSW condition code before the PSW is stored).
2. It causes repetitive looping through the validate microprogram until system reset is depressed.
3. It is used in conjunction with Y3 for I/O microprogram interrupts and I/O interrupts of machine-language programs.

Y3 (Y3 Stat)

This indicates the on/off condition of the Y3 stat, and is used for multi-purpose system operations. (See "YA Stats – Y2".)

YB Stats

These are used as general-purpose stats that serve as temporary storage for the microprogrammer.

They can be set or reset, individually or collectively, by the microprogrammer to recall the result of a test or operation performed during a previous microprogram step. It can then be tested later to perform a microprogram branch.

Y4 — Y5 — Y6 — Y7

These indicate on/off conditions, and are used as general-purpose stats.

They can be set or reset from the emit field or from the console data keys.

System reset resets all YB stats.

YD Stats

These can be set or reset from the emit field or from the console data switches.

ID (Inhibit Dump — Y8)

This indicates on/off condition of the inhibit dump stat.

When on, this stat prevents a dump operation from occurring.

MI (Maskable Interrupt — Y9)

This indicates on/off condition of the MI stat.

When on, this stat generates a PRI branch on the next I-fetch.

MAN (Manual Stat — Y10)

This indicates on/off condition of the manual stat.

It permits manual loading and displays of registers and storage.

It alters the meaning of specific microinstruction control fields for certain manual operations, and permits error resetting under microprogram control (CR field = 6).

It is used in log out.

Emulator Stat-Y11

The Y11 stat is used when the system operates with an emulator program.

Y11 is on for a 1401/1460 program.

Y11 is off for a 1410/7010 program.

The Y11 stat sets ROS address bit 11 which causes the 1401/1460 ROS modules to be addressed. The 1401/1460 ROS modules are 16-23 if the 1410/7010 emulator is *not* installed an 24-31 if the 1410/7010 emulator is installed. The 1410/7010 emulator always occupies modules 16-23.

YE Stats

Error Stat (Y12)

This indicates on/off condition of the manual stat.

When on, the Y12 stat prevents dump routines from being initiated.

It is during internal ROS diagnostics and microprogram log out, and is reset by microprogram (CN field = 9).

The error stat (if enabled) is set by detection of any condition that causes a log out. Once the error stat has been set, the detection of any other error results in a hardstop, except during microprogram log out when only a control check forces a hardstop.

IZT/IDQ (Integrated Zero Test/Invalid Decimal Digit on Q Bus — Y14)

This is the OR of IZT and IDQ conditions.

IZT is the latched condition of an ALU nonzero output to retain the ALU $\neq 0$ test for several cycles.

Y14 cannot be set from the console.

IDQ indicates an invalid decimal digit is on the Q bus.

LOAD (Y15)

This is turned on by the pushbutton, and when on, an error forces a hardstop.

It also tells the microprogram to go from system reset to IPL.

Y15 lights the load light on panel H.

LOAD (Y15) is turned on by the load pushbutton, and turned off when the load PSW, stored in location 000, is loaded in the data flow.

ALU Control Indicators

These indicators show the state of the ALU control register that is used in indirect functions.

Skew Indicator

This indicates the on/off condition of the ALU skew control latch.

Skew Select Register Indicators

These indicators show the output of the skew register.

ALU Binary Output Indicators

These indicate ALU binary output before decimal correct.

They are connected to positive lines of 2-W check.

LSAR — H — J Indicators

These indicators operate in conjunction with the LSA bus display and store switch. (See "LSA Bus Display and Store Switch".)

They also indicate the contents of the LSAR latches.

These registers may be displayed:

LSAR register
H register
J register

ROBAR — ROSAB — ROAR — ROSCAR Indicators

These indicators show the contents of the ROBAR latches.

They operate in conjunction with the ROBAR display toggle and channel select switch (panel C).

These functions may be displayed:

ROBAR	Read Only Back-up Address Register
ROAR	Read Only Address Register
ROSAB	Read Only Storage Address Bus
ROSCAR	Read Only Storage Channel Address Register

Storage Toggle Switch (Stats/LSA)

This switch is active in the hardstop state.

Up Position — Stats

This generates MSS pulses.

Data keys content is transferred to YA, YB, YD and Y12, Y15 stats.

The YA, YB parity latch is correctly set.

Y14 (IDQ, IZT) stat cannot be changed.

This toggle switch places the content of the data keys into the Y stats, resetting first the original content. The system must be in hardstop state (T clock stopped).

Figure 17 shows the circuit. Note that the store toggle switch generates the MSS1 pulse (Figure 18). The hardstop-allows-display condition can be found in Figure 502.

Stat Y14 cannot be changed from the console because it is really two latches (IZT and IDQ).

The correct parity is automatically generated for the YA and YB stats, but bad parity can be introduced using the reverse-data-parity toggle switch in console panel C.

Down Position — LSA

This works with the LSA-bus-display-and-store rotary switch.

The store-LSA toggle switch generates MSS pulses.

Display and store of H and J is via LSA.

The store-LSA toggle switch works with the LSA-bus-display-and-store rotary switch in console panel C.

The LSA bus display and store rotary switch in its home (LSAR) position allows display of the local

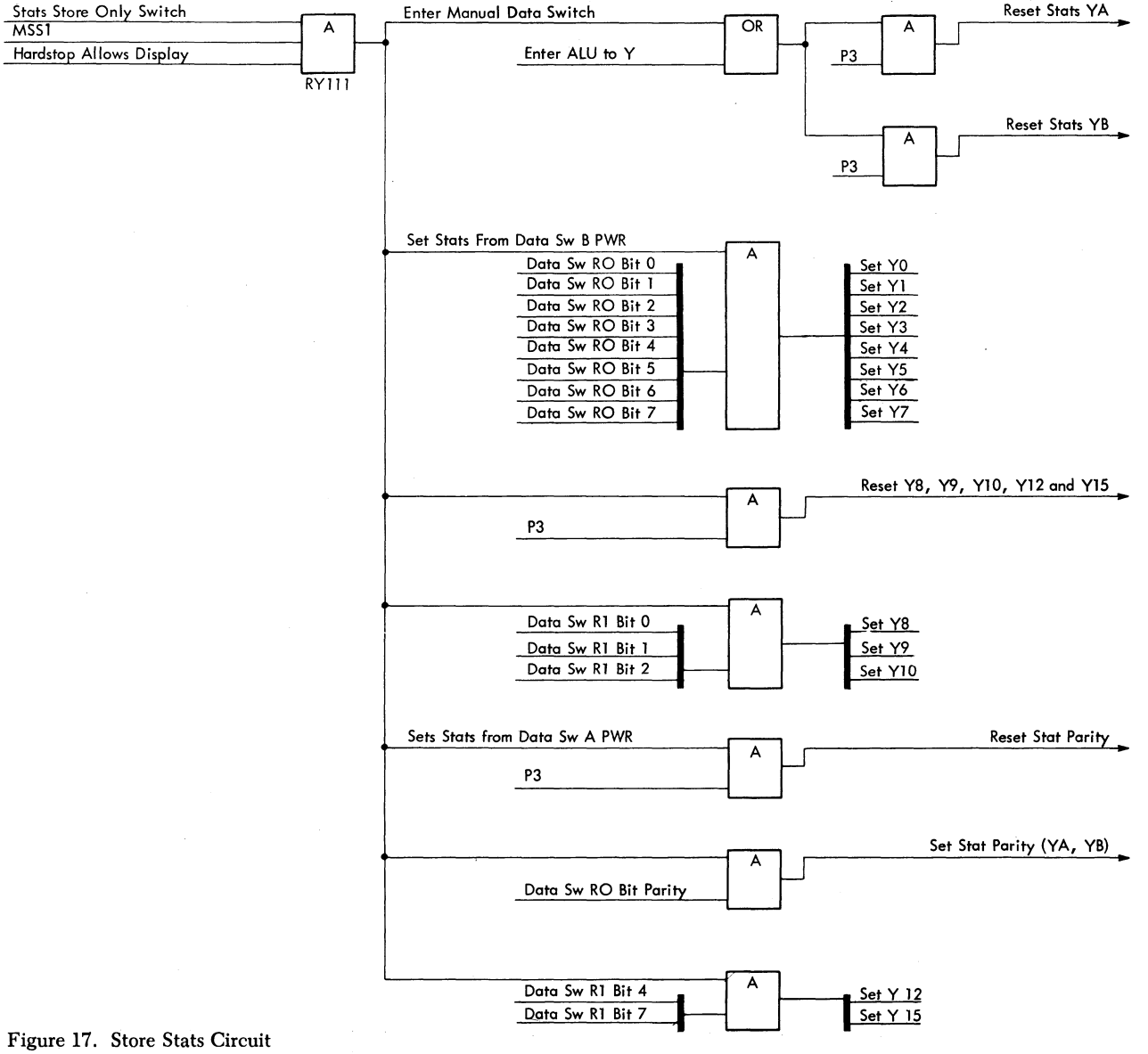


Figure 17. Store Stats Circuit

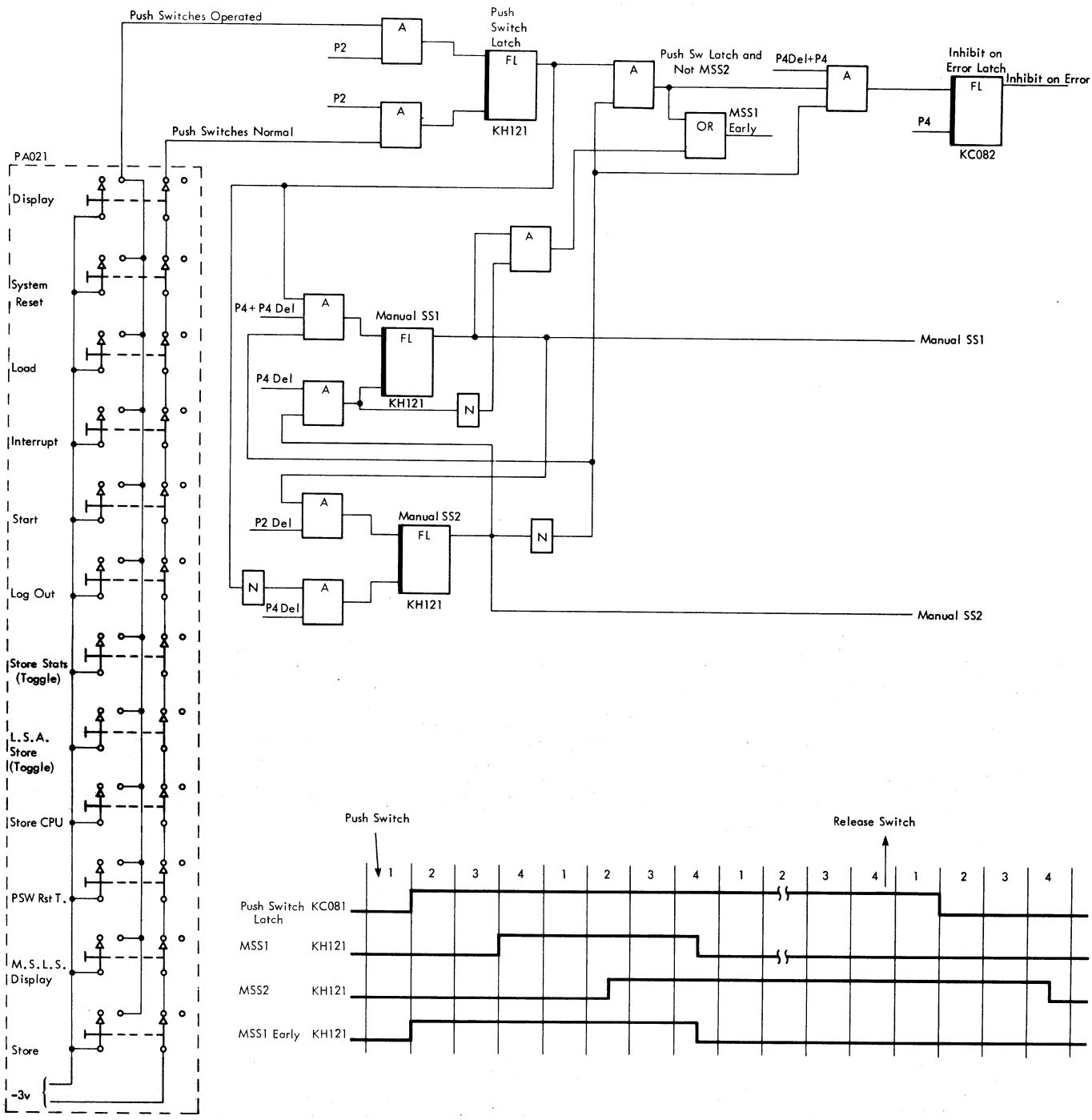


Figure 18. Manual Control Timing Ring

storage address register directly on the LSAR indicators.

Switching this rotary switch to the H or J position results in a transfer of the selected register into LSAR if the system is in the hardstop condition (Figure 19).

Whenever the rotary switch is in the H or J position and the store toggle switch is active, the content of the address switches is set into LSAR via the R register and transferred from LSAR via the local store address bus to the selected H or J register (Figure 19).

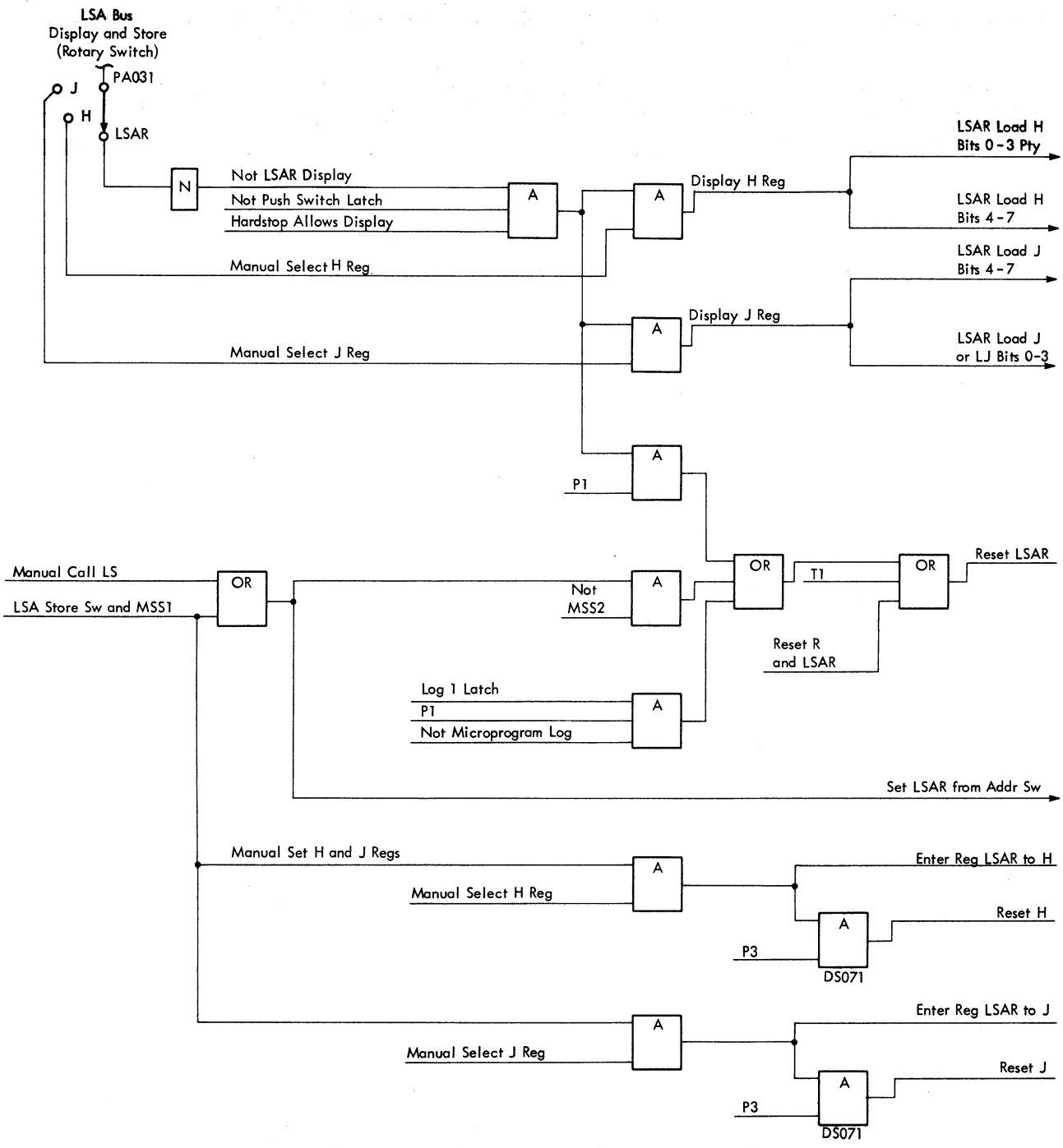
This setting of H or J register is obtained during the MSS1 pulse generated by the LSA-store toggle switch.

ROBAR Display Switch

This switch allows loading of ROBAR from: ROSAB, ROAR, ROSCAR1 or ROSCAR2.

The test light is active when this switch is not positioned to ROBAR.

The switch is active in the hardstop state.



KH 131

Figure 19. LSA Store-Display

NOTE: (1) The ROS address register may be displayed in control (ROSAB position), in ROAR, or in one of the ROSCAR registers. (2) Contents of ROBAR should be recorded before moving the switch off the ROBAR position.

Moving the switch down to ROAR/ROSCAR destroys the contents of ROBAR and forces the contents of ROAR or ROSCAR (selected by the channel select switch panel C) into ROBAR.

Moving the switch to the ROSAB position forces the contents of the ROS address register in control when the hardstop occurred into ROBAR.

Channel Display Switch

This switch operates in conjunction with:

1. The channel select switch
2. Display roller position 5

It is used for selector channel operation.

With the display roller switch in position 5, the channel display switch selects either the byte (T), or the buffer registers (W) for display. The channel select switch selects the desired channel. The channel protect key is displayed in the W2 register (bit positions 4, 5, 6, and 7 of byte 1).

NOTE: Registers W0 and W1 are reversed if the read backward bit is on; i.e. W0 in byte 1 and W1 in byte 0. The read backward bit (byte 0, bit 7) is displayed on display roller position 4.

Roller Toggle Switch

This switch operates with the store/display roller switch and the display roller switch.

It is active in the hardstop state.

Store

This allows store operations of registers, local storage, and main storage.

Display

This allows the display of positions 1 and 7 of the store/display roller switch and positions 6, 7 and 8 of the display roller switch.

Store/Display Roller Switch

This switch is active in the hardstop state.

It operates in conjunction with the roller toggle (store/display) switch and the channel select switch (panel C).

The selected register is gated directly into the R register for display, using the not real time clock drive line.

It enters information or data on the bus from the data keys when in a store operation.

Address keys are used to address particular local and main storage locations while the data keys provide the means of entering new data.

The manual set R register line is developed to gate the store display roller information to the R register alternately with the display roller information. The real time clock display gate controls the gating to the R register (Figure 20).

All selected positions of the display roller are gated with the same manual set R register display line.

The store/display roller switch uses the manual set R register display and store line for gating the selected register into R (Figure 20).

Whenever the roller toggle switch is set to the display or store position, the manual store or display latch is turned on for six microseconds. The gating of the display roller selected register and the store display roller selected register is stopped during the time the push switch latch is on. This allows setting of the address and/or data key content into the R register, and from there to the selected register.

Whenever MS or LS is selected an additional latch is turned on to develop the signals, manual read MS or manual read LS.

NOTE: Unless the store/display roller switch is set to the LS/R register position when a hardstop is encountered, the contents of the R register are destroyed. The correct procedure is to set the display switch to the LS/R register position, unless actual store/display operations from the console are being performed.

Roll Chart – Upper (Figure 15)

This chart allows viewing the data outlined in each section.

These indicators displayed by the chart are connected to the R register but gated with the real time clock display gate. They are used to display via the R register, the register selected by the upper roller switch.

1. The selected register is gated directly into the R register, or via the Q register, into the R register.
2. The R register is shared between display roller and store/display roller.
3. The real time clock display gate is used to gate alternatively the display and the store/display selected register into R.
4. The roller toggle switch is used in conjunction with roller switches.

The display roller switch gates different selected registers on display. The second and fifth positions of this switch are used with the channel-select rotary switch to display SC1 or SC2 registers. Position five is additionally gated with the channel display rotary switch to select various selector channel registers.

Figure 21 shows how, for positions 6, 7, and 8, the selected register is gated into the Q register with the MSS1 pulse generated by setting the roller toggle to the display position. The P register and extension are set to 0 with good parity.

Local Storage/R Register – Position 1:

1. Displays the contents of the R register (roller toggle switch in neutral position).
2. Displays the contents of a particular local storage address as specified by the address keys (roller toggle switch in display position).
3. Stores data from the data keys to a particular local storage address as specified by the address keys (roller toggle switch in store position).

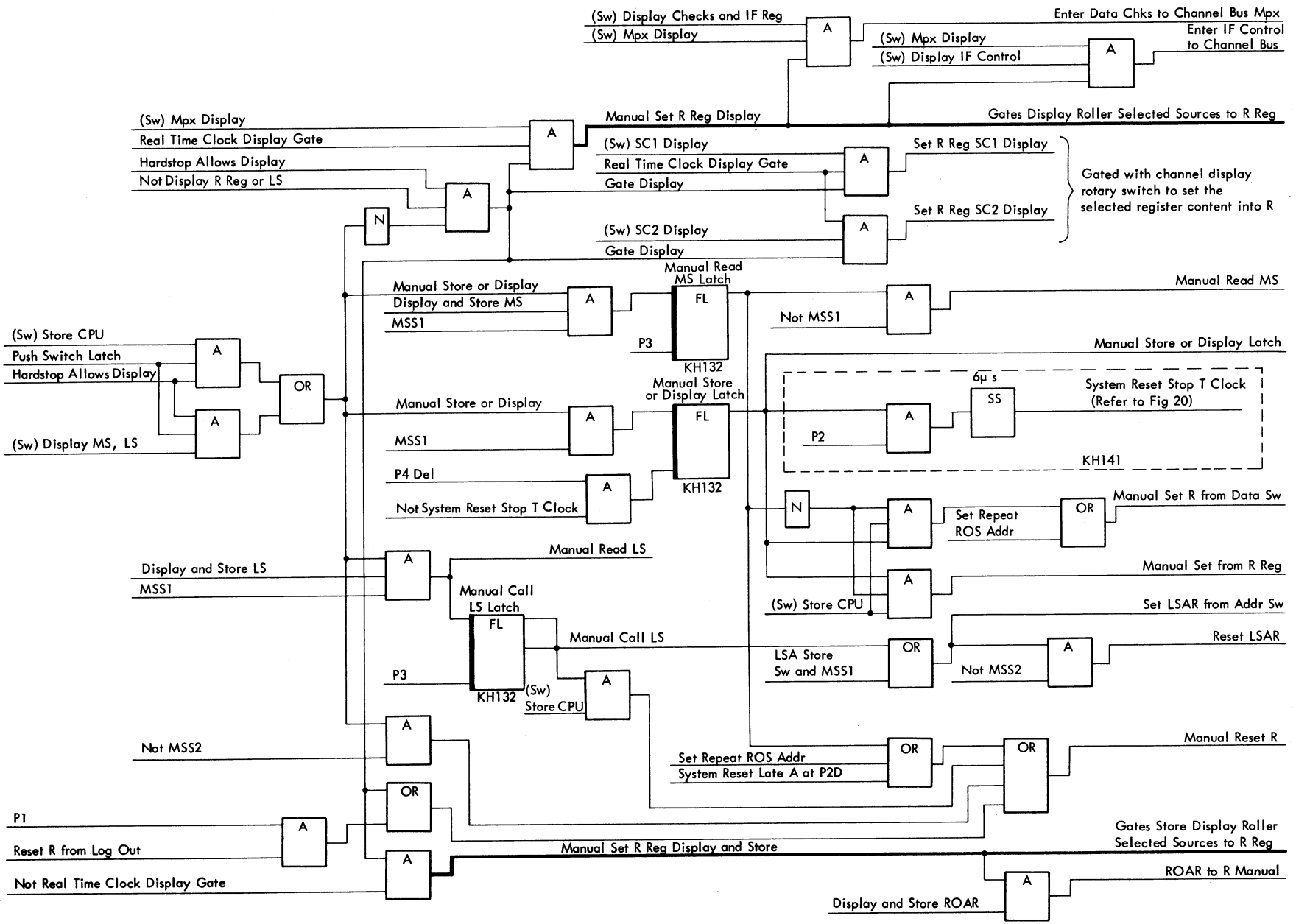


Figure 20. **Display and Store Display Roller Switches**

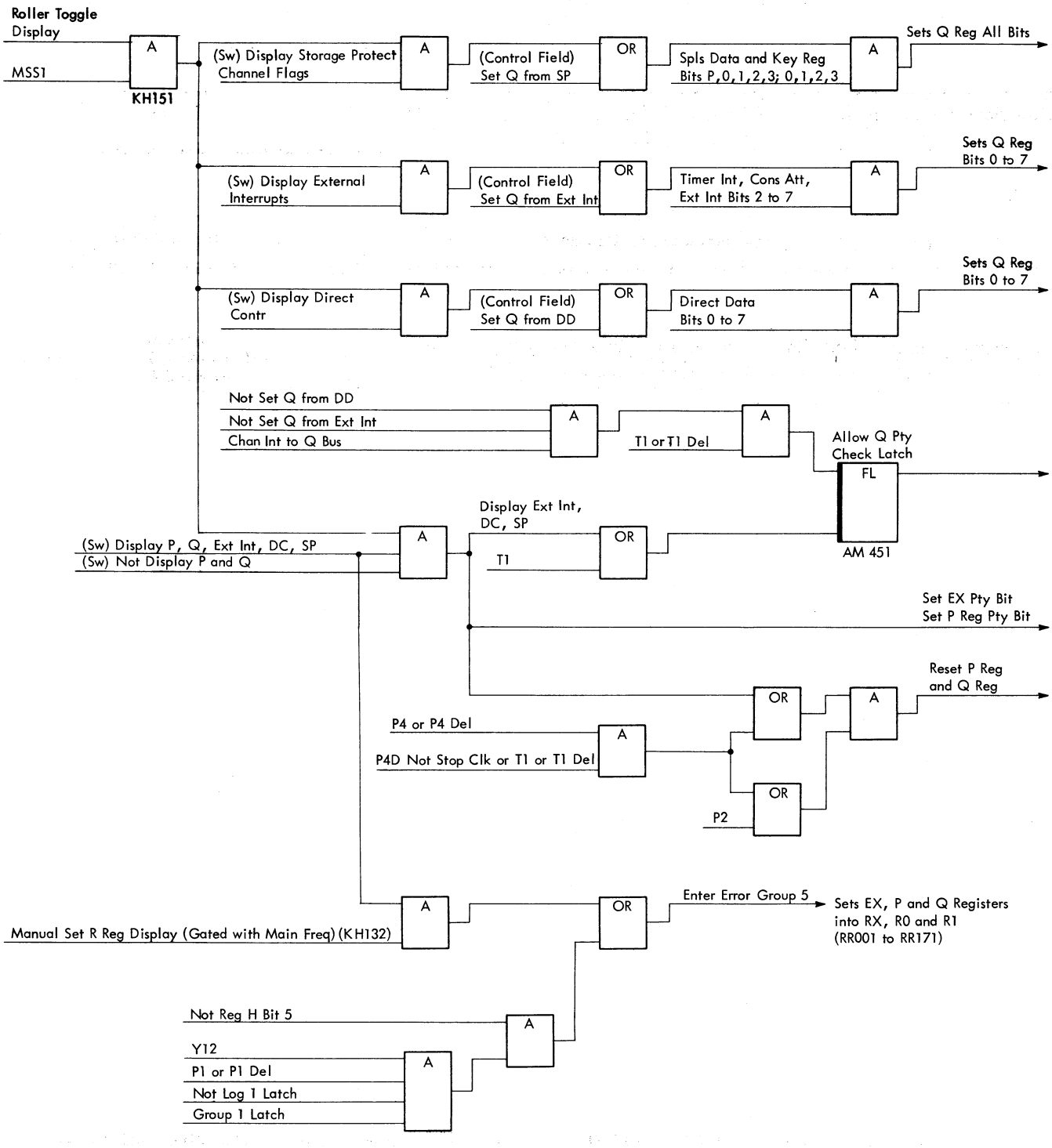


Figure 21. Display Roller Switch Positions 1, 6, 7, and 8

4. If the store display roller switch is on position 1 before stopping, the actual content of R register is displayed. In every other position, the content of the R register is destroyed.

NOTE: The setting of the store/display switch to position 1 prevents the display of the display roller switch.

A or S Register – Position 2:

1. Displays the contents of the A or S registers in the display indicators, depending on the setting of the channel select switch, Mpx or SC.

2. Stores data from the data keys into the A register regardless of position of channel select switch.

3. Data cannot be entered into the S registers from the data keys.

B Register – Position 3:

1. Displays the contents of the B register in the display indicators.

2. Stores data from the data keys in the B register.

C Register – Position 4:

1. Displays the contents of the C register in the display indicators.

2. Stores data from the data keys into the C register.

D Register – Position 5:

1. Displays the contents of the D register in the display indicators.

2. Stores data from the data keys in the D register.

Store ROAR – Position 6:

1. Displays ROSAB (0-11, CPU, ISA, and PSA latches) in the display indicators. Also displays ROSAB, bit 12 and DAT latch (RX003) in byte X, bits 6 and 7.

2. Transfers data key information (byte X, bits 7 and 6, to ROSAB (12) and DAT latch) to ROAR when the roller toggle switch is in the store position. Correct parity is generated. ROS data addressed by ROAR is now available in the CE panel lights.

3. Roller toggle switch is not active in the display position.

4. Parity bits displayed are byte parity bits. ROAR parity is not displayed.

Main Store – Position 7:

1. Not active with the roller toggle switch in central position.

2. Roller toggle switch to display – forces main storage cycle using contents of storage address keys to address. Data from this address are displayed in the storage data lights on panel F.

3. Roller toggle switch to store – forces main storage cycle using contents of storage address keys to address main storage. Stores data from storage data keys in main storage. This data is displayed in indicators and also in the storage data lights on panel F.

NOTE: The original contents of A and D registers are destroyed if the machine is hardstopped and any S to SAB light (panel A) is lit. Storage address keys are used to set A register as normal but relative S register is used to address main storage.

4. Used in conjunction with Mpx stor key to address multiplex storage.

Display Roller Switch

This switch is active in the hardstop state. It displays contents as outlined in the detailed description of the roll chart given in Figure 16.

NOTE: (1) The contents of P and Q are destroyed when positions 6, 7 and 8 of this switch are displayed (Figure 21). (2) If the store display switch is positioned to the LS/R position, the display roll switch is disabled. Move the store/display roller switch off the LS/R position to activate the display roller.

Roll Chart – Lower (Figure 16)

This allows viewing data outlined in each section without further console lights.

These indicators are connected to the R register but gated with the real time clock display gate (Figure 20). They are used to display, via the R register, the register selected by the lower roller switch.

ALU EX, P and Q – Position 1: This displays registers EX, P and Q, in bytes X, 0 and 1 positions of the display lights.

NOTE: With the roller toggle switch in the display position and the display switch set to either external interrupts (6), SP data and key (7), direct control (8), the original contents of EX P and Q are destroyed.

Checks and IF Register (Checks and Interface Registers) – Position 2:

1. Displays the selected channel checks in byte 0 and the multiplex channel interface bus-in or selector channel errors in byte 1 (depending on the position of the channel select switch).

2. The channel displayed is dependent upon the channel select switch (console panel C).

NOTE: The red area of the roll indicates error conditions.

IF Controls (Interface Controls) – Position 3: This displays the IF controls of the channel selected by the channel select switch (console panel C).

Channel Controls – Position 4: This displays the channel controls of the channel selected by the channel select switch (console panel C).

The format for the selector channel is shown in Figure 16.

Channel Registers – Position 5:

1. Operates with the channel display switch.

2. Displays selector channel byte count, buffer registers and channel key.

3. When the channel display switch is in the W2 position, W2 is displayed in byte 0 and the channel key is displayed in byte 1 positions P, 4, 5, 6, and 7.

4. T0, T1, W0, and interface bus-in are parity checked.

NOTE: If the read backward bit is on (visible at position 4, channel controls) then W0, W1 are displayed backwards.

On an input operation (read or sense) W0 and W1 feed R0 and R1 respectively on the R bus. On a read backwards operation, W0 and W1 feed R1 and R0 respectively on the R bus. Consequently W0 and W1 are grouped together for visual display since they operate closely together.

On an output operation, write or control, W3 and W4 are fed from the D register via the R bus. Consequently W3 and W4 are displayed together just as W0 and W1 are. Forward interface is fed into the W4 register for both a read and write operation.

External Interrupts — Position 6: This displays external interrupt latches in the display indicators via the R and Q bus.

SP Data and CPU/Channel Key (Storage Protect Data and Key) — Position 7: Displays data and key registers as described below.

The contents of the storage protect data register are displayed in bits 0-3 of byte 1. The contents of the CPU or Mpx channel storage protect key register are displayed in bits 4-7 of byte 1. These displays occur via the R and Q bus.

NOTE: SC key is not displayed in this position.

Direct Control — Position 8:

1. The contents of the direct control accept register are displayed in byte 1 of the display lights.
2. Data flow is via the R and Q bus.

Console Panel F

Whenever the keys are used with the address-compare rotary switch (console panel G) the address-key contents are compared with the main storage address bus, and the data-key content with the read only storage address bus.

The reverse data parity toggle switch is provided to transfer bad parity from the storage data keys to the R register or to the Y stats (ALD PA001).

Address Keys

The address keys are used with:

1. Storage select switch (console panel G) when in manual state.
2. Store/display roller switch, and the roller toggle switch when in hardstop.
3. LSA bus display and store switch (console panel C) and the store switch in LSA (console panel D) when in hardstop.

The correct byte parity is automatically generated, and keys are active (binary one) when down.

Data Keys

Data keys are used with:

1. Storage select switch (panel G), in manual state.
2. Store display roller switch and roller toggle switch (panel D) when in hardstop.
3. Store toggle switch (panel D) for storing stats when in hardstop.

Correct byte parity is automatically generated and keys are active (binary one) when down.

Instruction Counter and Storage Address Indicators

Extension bit 7, byte 0 bits 0-7 and byte 1 bits 0-6 are driven directly from SAB. Byte 1 bit 7 and extension bits 5 and 6 are driven directly from A or S register, depending on which register is forcing SAB.

SAB is driven from S register bit-for-bit when the channel control reinterpret latch is active. SAB is driven from A register with the bits displayed to form Mpx storage address when UBA (Y1) stat or Mpx storage key (panel C) is active. SAB is driven from A register bit-for-bit at any other time.

NOTE: S to SAB lights on panel A help in determining the source of SAB. SAB/P parity indicator refers only to SAB; therefore, extension bits 5 and 6 and byte one bit 7 should be disregarded except in the case of a 256K storage when only extension bit 5 and byte one bit 7 should be disregarded.

Storage Data Indicators

These indicators directly display the contents of the D register.

They are used to display data from various sources within the IBM 2040 by loading the D register with the desired information.

Console Panel G

Pushbuttons and Switches for Generating MSS1, MSS2

There are three manual singleshot (MSS) pulses: MSS1 early, MSS1 and MSS2 (KH121). These are generated when pushbuttons or toggle switches are pressed, and are used to gate sets and resets on latches controlled by pushbuttons or toggle switches.

Eight pushbuttons and two toggle switches set the

push-switch latch when they are activated (Figure 18). The push-switch latch is turned off at P2 after the switch is deactivated.

The following pushbuttons and toggle switches set the push-switch latch:

Load pushbutton
System reset pushbutton
Display pushbutton
Store pushbutton
Log out pushbutton
Interrupt pushbutton
Start pushbutton
PSW restart pushbutton
Store stats or LSA toggle switch
Store or display roller toggle switch

Each time the push-switch latch is set, three pulses (MSS1 early, MSS1, and MSS2) are generated (Figure 18) and all latches that can be set or reset from the console are gated with one of these pulses.

MSS2 is an interlock latch to prevent more than one MSS1 pulse.

Stop Pushbutton

(See Figure 22 and Figures 013 and 014.)

- **Pressing the stop pushbutton causes the microprogram to enter the stop loop at start of next I-fetch.**
- **The machine instruction in progress is completed.**
- **The T clock is not stopped.**
- **All pending program interrupts are taken prior to stop loop entry.**
- **Start, display, store pushbuttons are active only in the stop loop.**
- **The manual light on the console (console panel H) is lit when the stop loop is entered.**
- **After entering the stop loop any I/O operation in progress is completed to the PRI scan.**
- **The display microprogram is executed prior to entering the stop loop.**

Pressing the stop pushbutton sets the halt latch, which forces a PRI branch condition in the next I-fetch routine. When the PRI branch is taken, the current PSW is updated and stored in local storage.

The start, display, and store pushbuttons are active to force a microprogram start address in ROAR only when the system is in the stopped state. (Figure 23.)

Whenever the stop pushbutton is pressed while an interrupt request is pending, the new PSW of the particular interrupt is first loaded as the current PSW before the stopped state is entered.

The current PSW in local store is always updated (condition code, high-order eight bits of the instruction counter and instruction length code) before entering the stop loop.

This stop loop is a one microinstruction loop in which the control manual is given. This control manual sets the manual latch to enable logic generation of ROS addresses (Figure 23). Normal channel operation is allowed in this stop loop.

If the stop key is pressed while the machine is in the wait loop, the same routines are executed. The wait latch, however, is not reset, resulting in wait and manual indications on the console.

The manual indicator comes on when the system is in the stop loop. The microprogram order manual is given, setting the halt-state latch (Figure 23).

Start Pushbutton

- **This pushbutton, when depressed in the manual stop state, forces ROAR to 400 (hex). Microprogram then loads PSW from local store into data flow and then to I-fetch if wait bit (bit 14) is not a binary 1 (QC071).**
- **When depressed in the hardstop state, the T clock is restarted and the next sequential microinstruction is performed.**
- **It is inactive when error conditions are present in process mode.**

Depression of the start pushbutton in manual stop state and not single cycle turns off the halt latch (Figures 18, 24 and 26). ROAR is forced to 400 hex (Figure 23) and the PSW is loaded into the data flow from local store; microprogram then goes to I-fetch via the wait loop. Processing proceeds with the execution of the instruction specified by the instruction counter. Depression of the start pushbutton in hardstop (single-cycle mode) allows any outstanding hardware cycles (log-out, dump, undump or trap) to be taken prior to starting the T clock. Following this, the microinstruction specified by the address in ROAR is fetched and the T clock started. Machine errors must be cleared or disabled before the start sequence can be initiated.

The start pushbutton is also used in single-cycle or instruction-step mode (see rate switch on this panel).

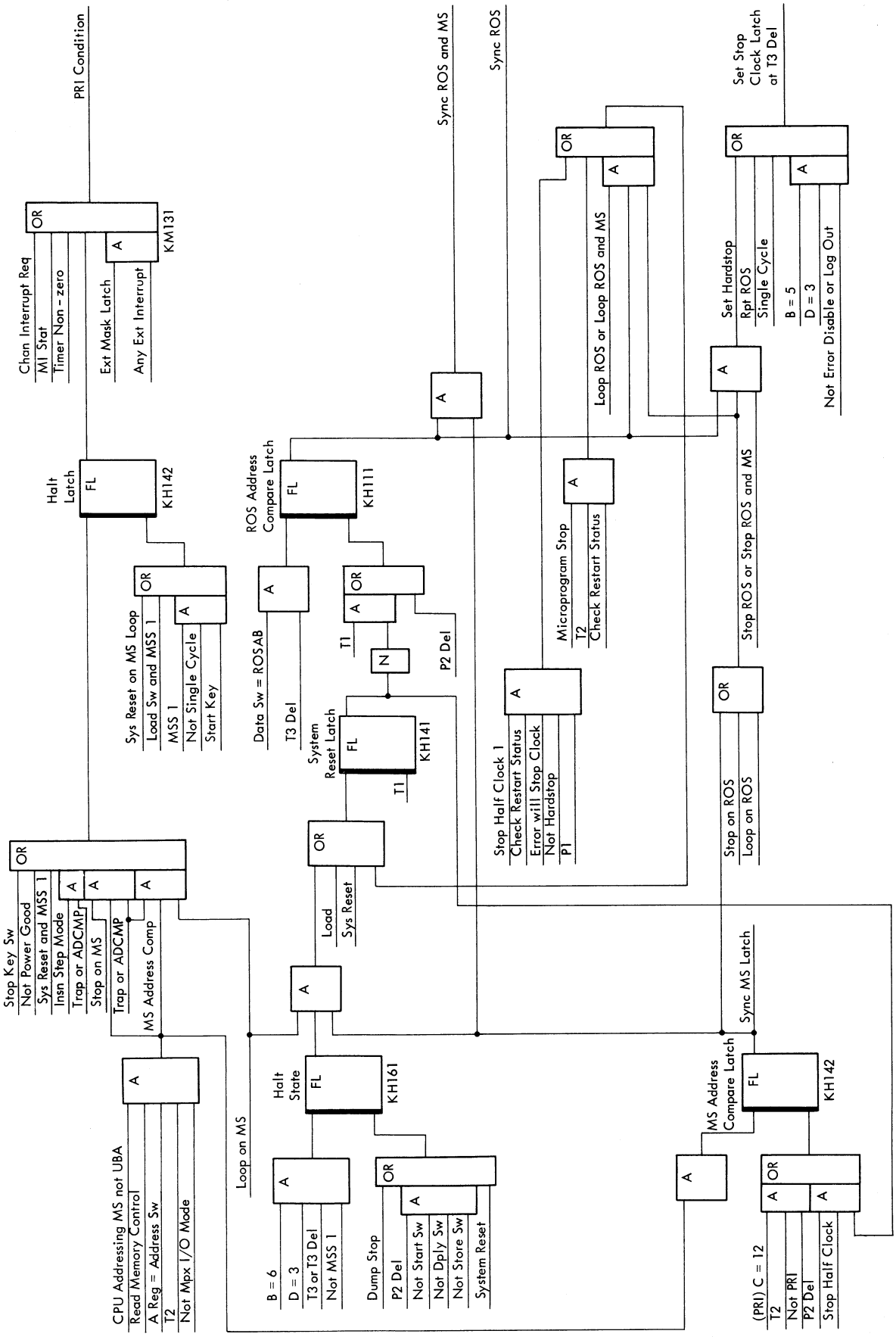


Figure 22. Address Compare Switch

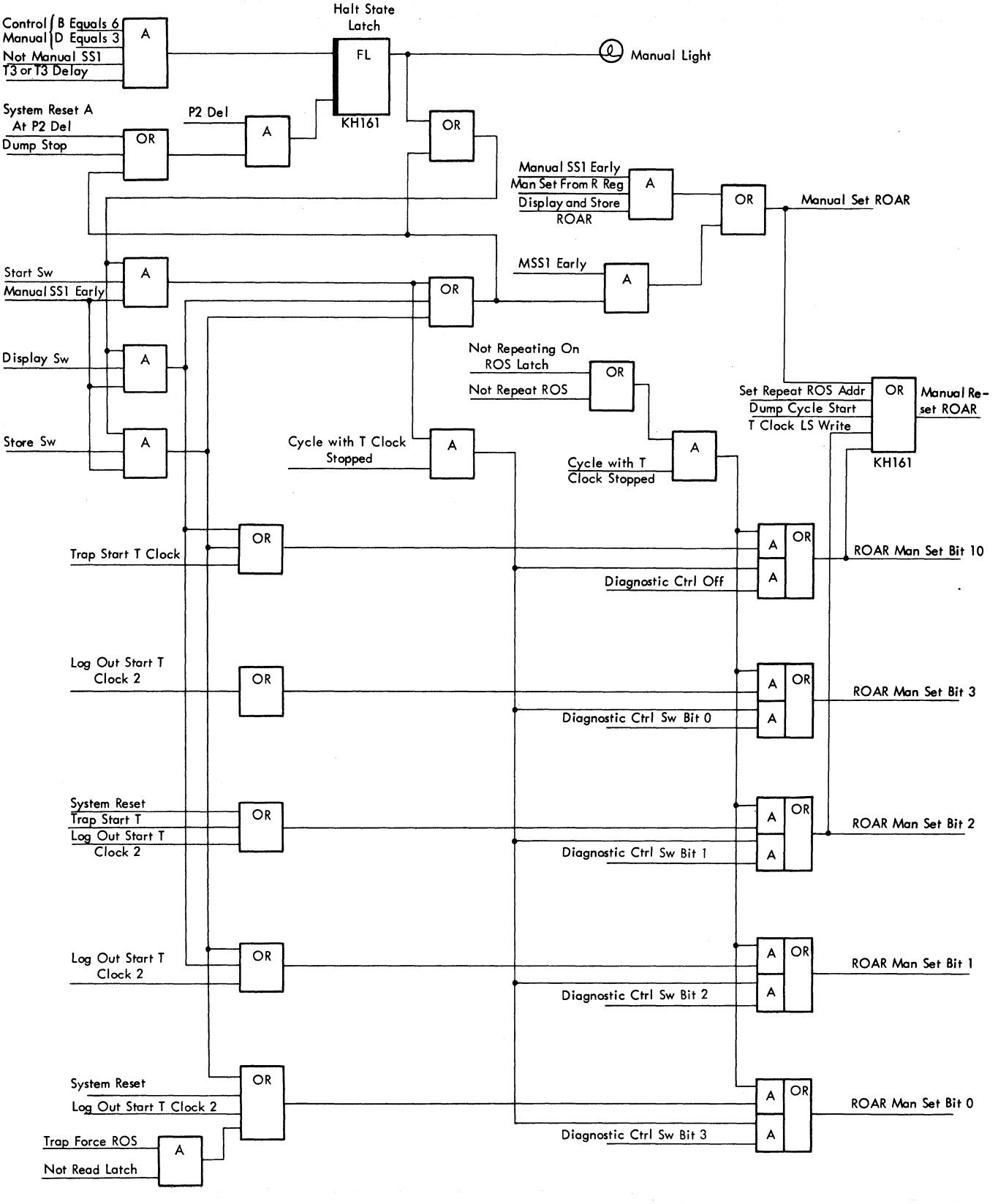


Figure 23. ROAR Forced Address

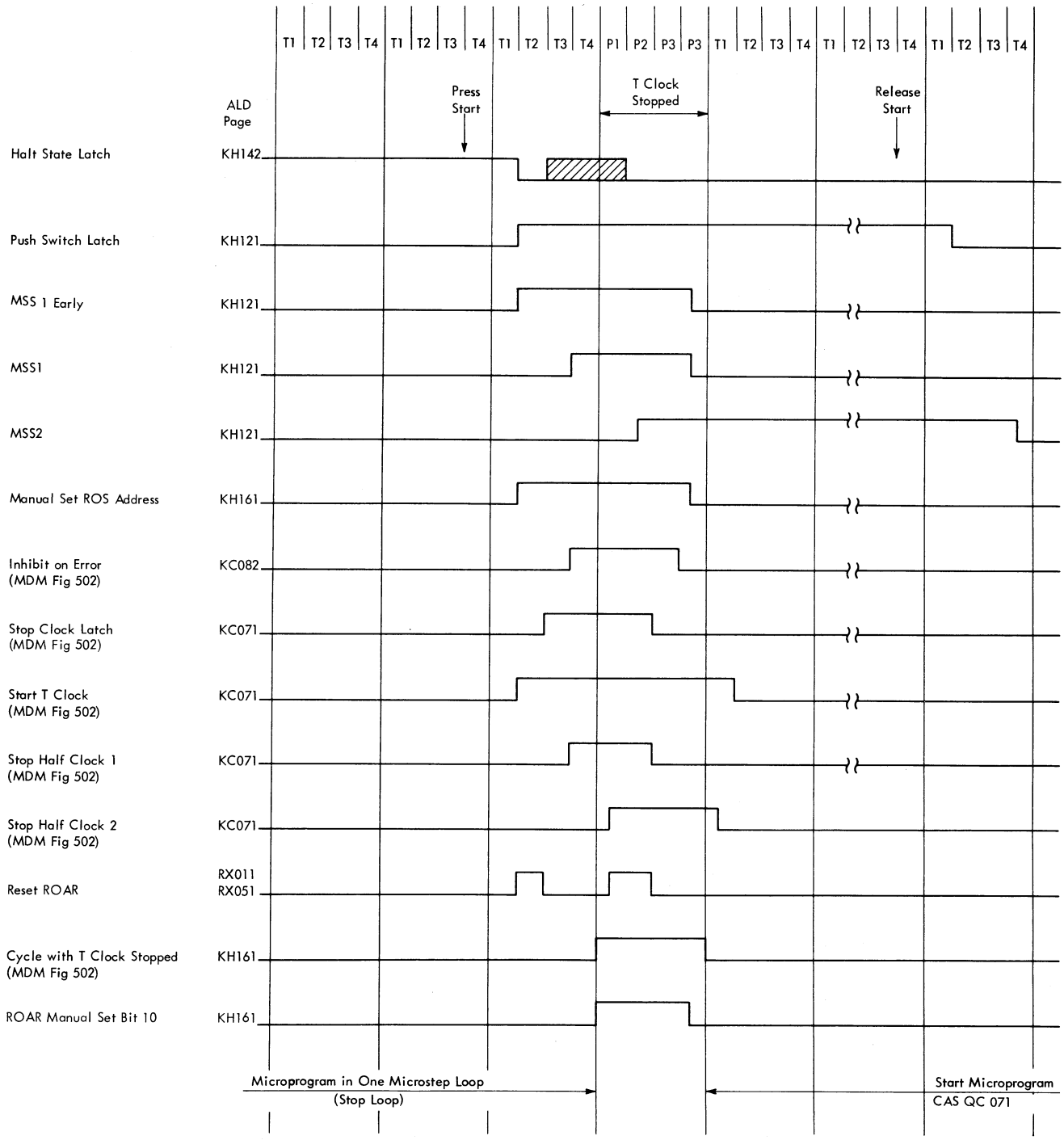


Figure 24. Start Button Sequence

Check Reset Pushbutton

- **Pressing the check reset pushbutton resets all CPU and channel error latches.**
- **The pushbutton is operative in all modes.**
- **The check reset pushbutton does not correct conditions which caused the error.**
- **Check lights remaining on after check reset has been pressed must be cleared manually at their source as certain errors will hold their checking circuit and the related error latch set.**

NOTE: In some cases, it is not possible to clear the error conditions manually (those items listed on the display rotary switch on panel D).

Exactly the same error reset lines are activated if the microprogram order 0 → ERR (CR = 6, Y10 = 1) is given or the system-reset pushbutton is pressed.

Note that only the error latches are turned off; as soon as the check-reset pushbutton is released, an error check latch may turn on again because the error is not cleared at the source.

These check latches are reset:

	ALD
LS read check latch	KH 025
Master check latch	KH 401
Late check latch	KH 401
Early data check latch	KH 401
Control check latch	KH 401
ROS address check	RX 001
P Field decoder check	DR 431
Q Field decoder check	DS 015
H Field decoder check	DS 081
RX check, R0 check, R1 check latch	KH 411
Diagnose or Y8 error	KM 121
IF control check SC1	GG 543
Channel control check SC1	GG 543
Buffer data check SC1	GG 543
Multi tag check SC1	GG 543
Bus in data check SC1	GW 509
W0 parity check SC1	GW 509
IF control check SC2	HG 543
Channel control check SC2	HG 543
Buffer data check SC2	HG 543
Multi tag check SC2	HG 543
Bus in data check SC2	HW 509
W0 parity check SC2	HW 509
IF tag check Mpx	FN 001
IF control check Mpx	FN 001
IF parity check Mpx	FN 011
Channel data check Mpx	FN 011
Channel control check Mpx	FN 011

Store Pushbutton

- **This is active only in the manual stop loop.**
- **Storage protect is not effective.**
- **Each depression of the pushbutton results in a single store sequence.**
- **It is used with the storage select switch, data and address keys, and indicators.**
- **A register is always displayed (via SAB) in instruction counter or storage address indicators.**
- **D register is always displayed in storage data indicators.**
- **It forces ROAR to the address of the store/display microprogram.**
- **Used to store data in a selected storage device.**
- **Parity lights refer to SAB or D register.**

See Figures 23 and 25.

Pressing the store pushbutton sets the error stat (Y12) and logic circuits force 403 into ROAR (Figure 24). This is the store entry to the store/display microprogram. The microprogram then sets enable to a binary 1 to allow Y12 to force a hardstop on errors. The CPU channel key register is set to zero by the microprogram whenever a read MS cycle is forced. This means that the SP feature is not effective when using this pushbutton.

NOTE: Contents of A, D, R and LSA registers are destroyed.

Display Pushbutton

- **Storage protect is not effective.**
- **Active only in the manual stop loop.**
- **The A register is always displayed (via SAB) in storage address indicators.**
- **The D register is always displayed in storage data indicators.**
- **This pushbutton is used with the storage select switch, data and address keys, and indicators.**
- **It forces ROAR to the address of the store/display microprogram.**
- **It is used to display data from a selected storage device.**
- **Parity lights refer to SAB or D register.**

Pressing the display pushbutton sets the error stat (Y12) and the logic circuits force ROAR to 402 (Figure 23). This is the display entry to the store/display microprogram. The microprogram then sets enable to a binary 1 to allow Y12 to force a hardstop on errors.

NOTE: This pushbutton is the singleshot type (i.e., for each depression, only one display operation will take place). Contents of A, D, R and LSA registers are destroyed.

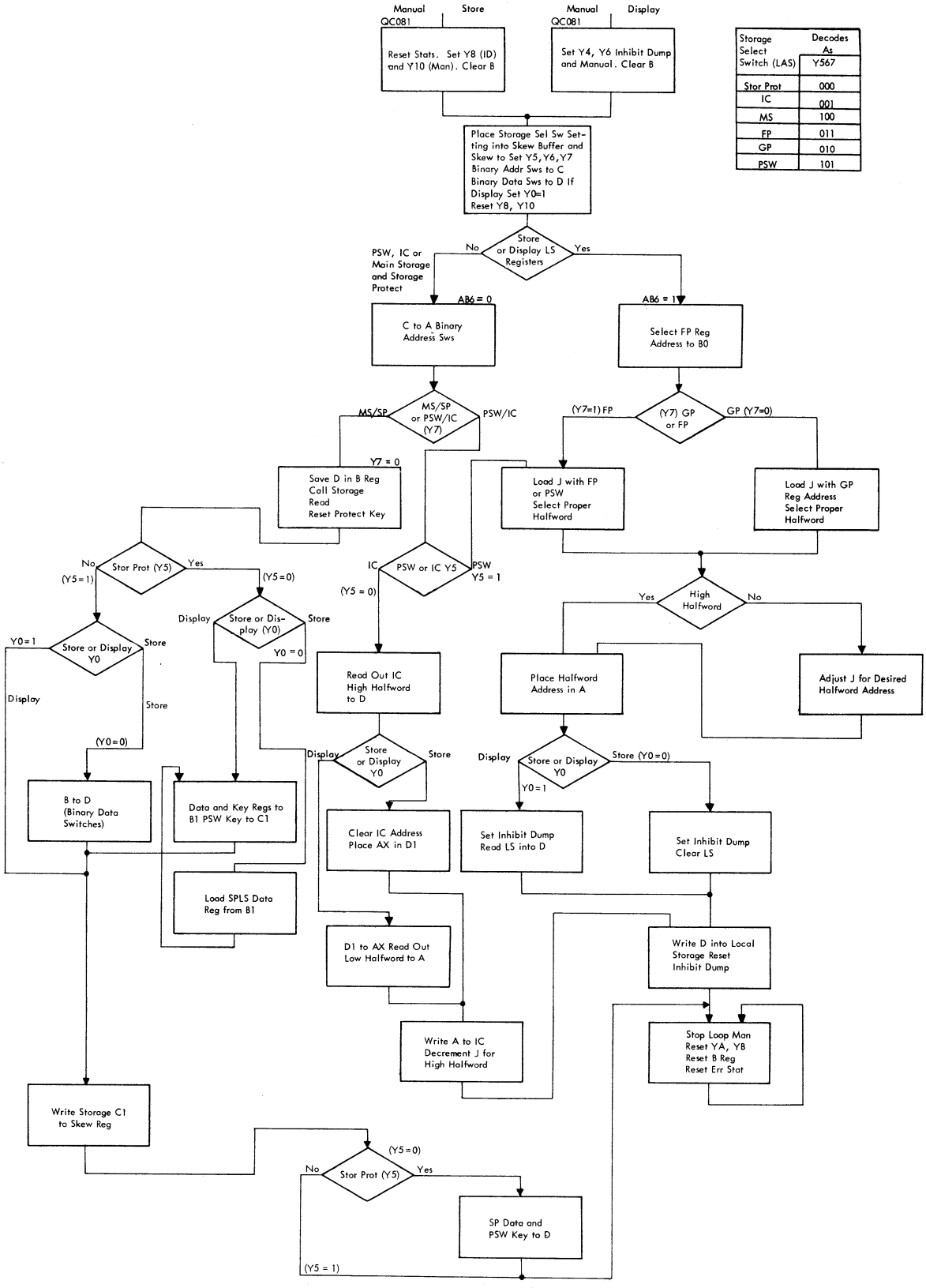


Figure 25. Manual Store and Display

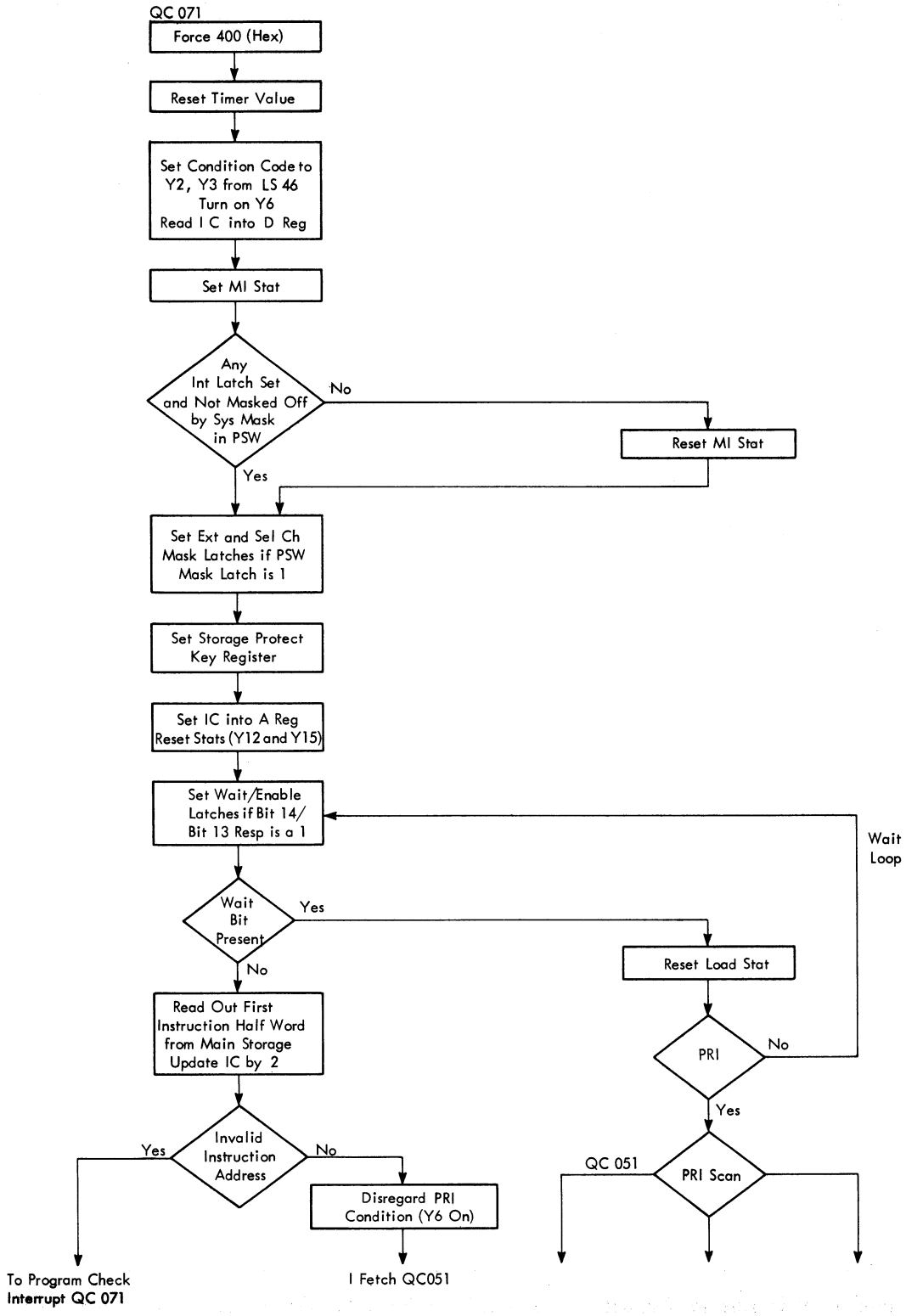


Figure 26. Microprogramming Initiated by Start Pushbutton

Log Out Pushbutton

- **May be used to force an exit from a microprogram loop caused by a machine malfunction.**
- **Stops the T clock and initiates a normal log out operation.**
- **Effective in all modes if Y12 is off and PSW bit 13 = 1 (system is enabled).**
- **Simulates machine error handling by forcing a machine check interrupt.**

NOTE: Since Y12 must be off prior to log out operation, this pushbutton is not usable during the execution of internal diagnostics, IPL, or the log out microprogram itself (Figures 013 and 014).

Pressing the log out pushbutton forces the start log latch and the stop clock latch on. These two latches stop the T clock and force a log out to take place. CPU checkout and system reset are executed and a machine check interrupt forced. In some cases, the stop pushbutton may be ineffective because of a machine malfunction which prevents the microprogram from reaching a PRI test. Under these conditions, the log out pushbutton may be used to stop the machine, force a log out, and load the machine check PSW to initiate the error subroutine specified by the PSW.

Refer to "Log Out" for a detailed description.

CE Lock

- **Requires a special key to operate.**
- **Selects customer or customer engineer meter operation.**
- **Test lamp is lit when in the customer engineer position.**
- **Key cannot be removed in customer engineer position.**

System Reset Pushbutton

- **Pressing the system reset pushbutton resets the CPU, channels and control units to their initial state.**
- **System reset consists of the sequential execution of a hardware system reset, CPU check out and microprogram system reset.**
- **This pushbutton is active in all modes.**

See Figures 27, 28, 29, and 30; also, Figures 013 and 014.

Pressing the system-reset pushbutton resets the system partially by logic circuits (hardware system reset), partially by microprogram (microprogram system reset). Between the hardware system reset and the microprogram system reset, the CPU and channel check-out microprogram is executed. The system enters the stop loop through the display microprogram routine at the end of the microprogram system reset.

For the over-all sequence, refer to the microprogram data flow, *Comprehensive Introduction, Field Engineering Manual of Instruction,* Form 223-2840.

The error stat Y12 is forced on during the hardware system reset, resulting in a hardstop condition whenever the system detects an error in performing the microprogram sequence previously mentioned.

The T clock is stopped during hardware system reset, but the gated T clock is kept running; this resets various latches in the selector channel hardware where, in general, gated T clock pulses are used. For example, on ALD page GG522, the bus-in-to-W4 latch is reset with gated T4.

Hardware System Reset (Figure 29):

1. Resets circuitry not accessible by microprogram.
2. Resets registers initially needed during CPU checkout.
3. Hardware system reset is active for 6 microseconds.
4. The first microinstruction address of CPU checkout is forced into ROAR.
5. T clock is stopped, gated T clock is running.

The following areas are affected by hardware system reset:

Reset registers A, D, SP data and key
Reset channels
Set the error stat (Y12)
Reset all other stats
Reset errors
Set enable
Reset hold latch and external interrupts
Reset all latched conditions
Reset channel interfaces

Operating the system reset pushbutton forces a hardware reset of certain areas, followed by a CPU and selector channel checkout, a microprogram system reset, and finally entry to the manual stop loop. If the main storage (MS) read latch is on when system reset is initiated, a MS write is forced, to prevent loss of MS data. During the hardware system reset, these steps are executed:

1. The halt latch is set to force an entry to the manual stop loop following the system reset microprogram.
2. The system reset latch is set. This stops the T clock and defines the hardware system reset.
3. The T clock is stopped for approximately 6 microseconds but the gated T clock keeps running.

NOTE: This is done to allow sufficient time for latches to be reset. A gated oscillator is used as a singleshot to time this operation.

4. The A and D registers, storage protect key and data registers are reset.
5. All stats, error latches, and external interrupt latches are reset.

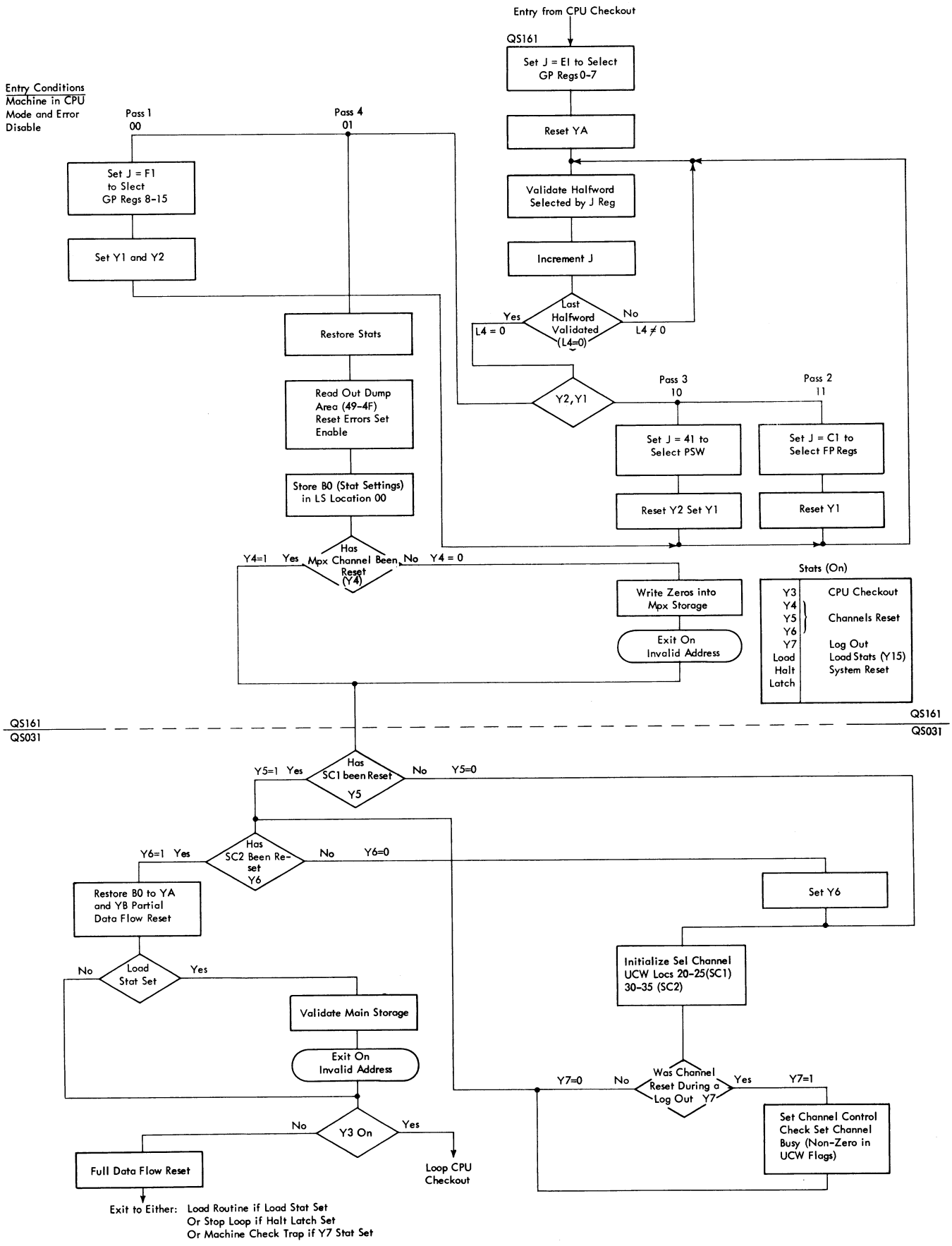


Figure 27. System Reset Microprogram

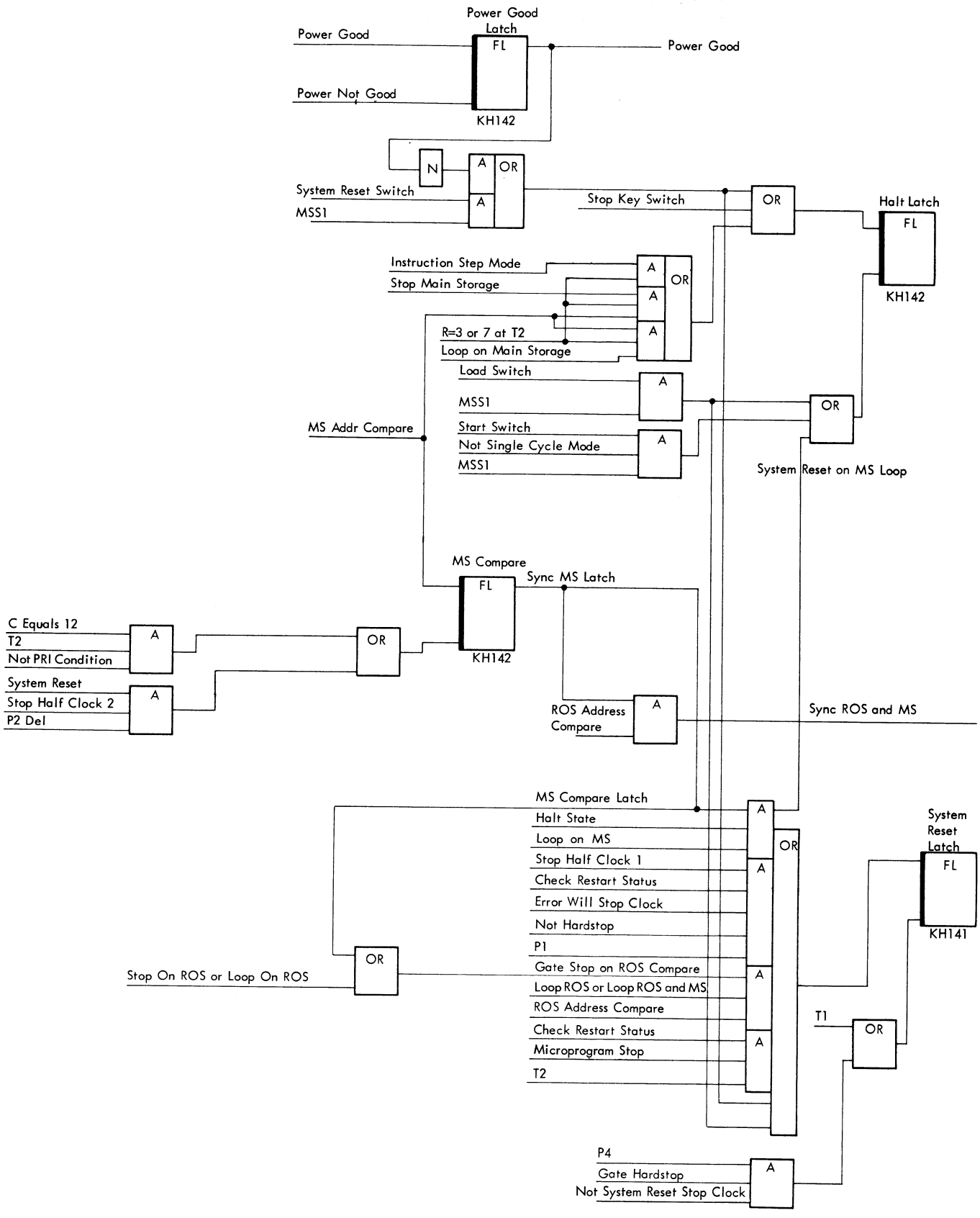
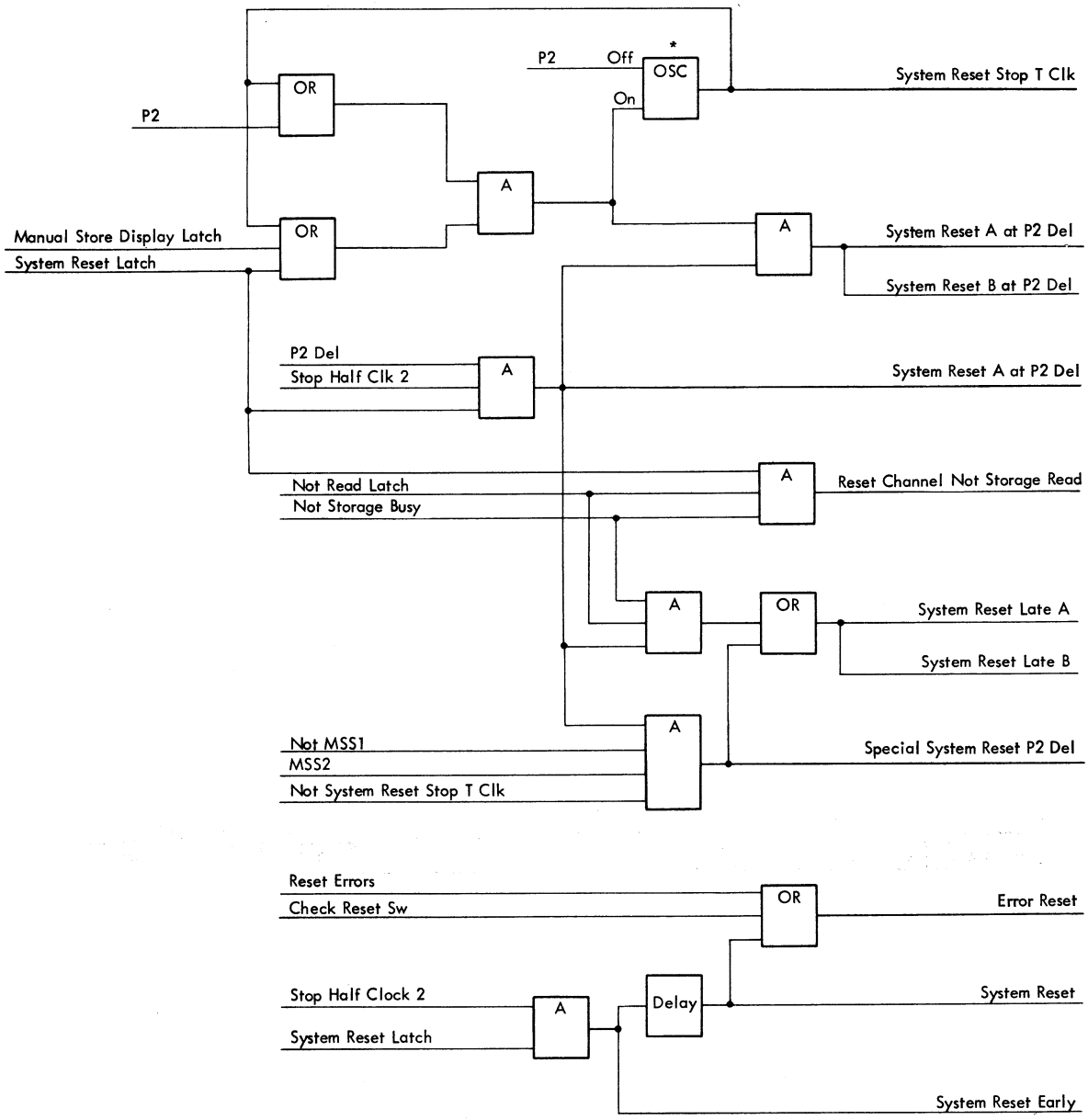


Figure 28. System Reset Latch



* Osc is used as a singleshot. The output of the Osc block rises with the On input and falls at P2 (Off input) following the end of one cycle. The time for one cycle is about 6 usec.

KH 141

Figure 29. System Resets

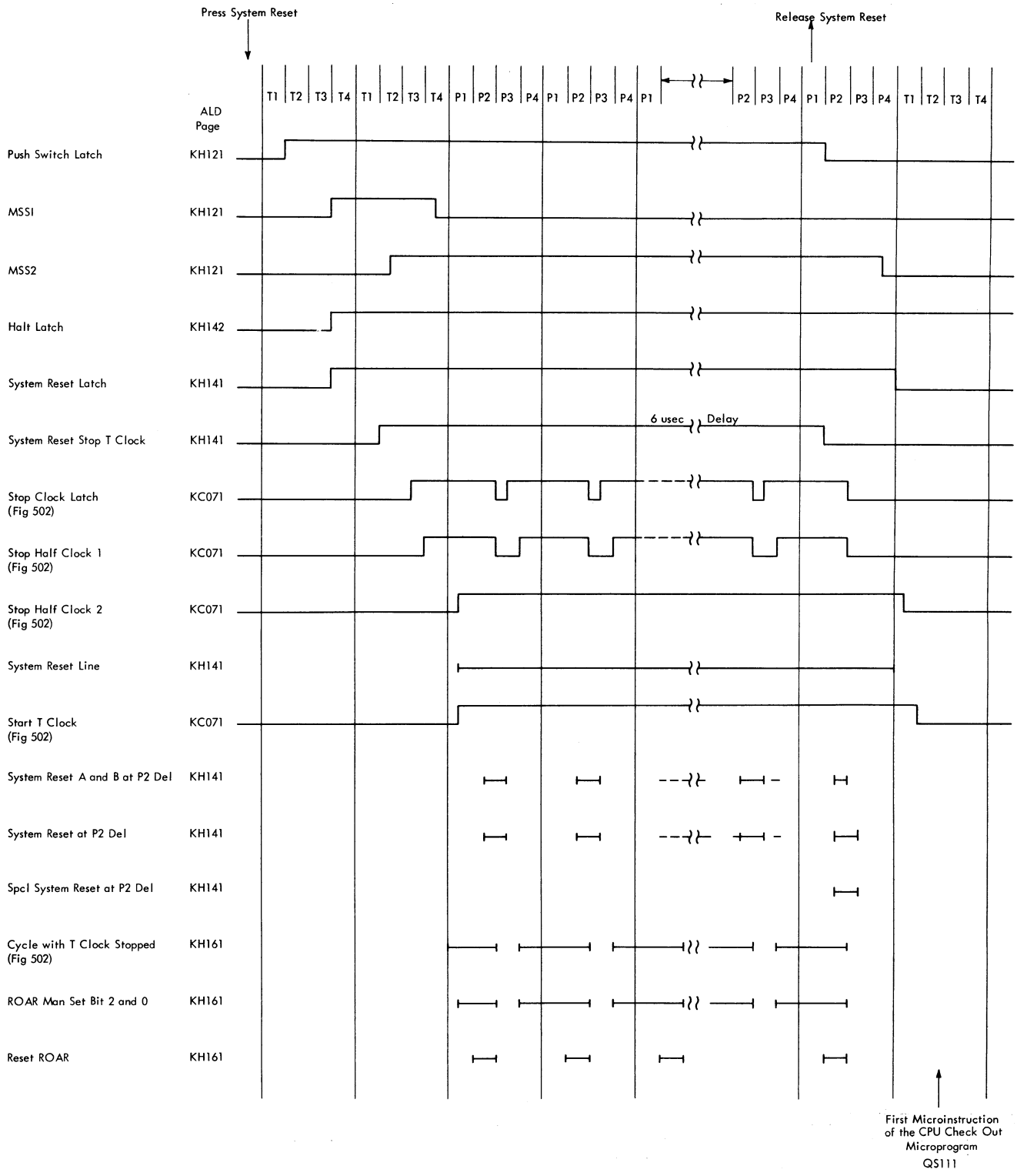


Figure 30. Hardware System Reset Timing Chart, Sheet 1 of 2

HARDWARE SYSTEM RESET

System Reset Latch forces following reset lines.

KH1H1

ERROR RESET which forces

FK051
- Clear Mpx Errors which resets
  - IF tag check
  - IF control check
  - IF parity check
  - Chan data check
  - Chan control check

GE581
- Clear SC1 Errors which resets
  - IF control
  - Chan control
  - Buffer data check
  - Tag check
  - W0 parity error
  - Bus-in parity error

HE581
- Clear SC2 Errors which resets
  - same as SC1

ERROR RESET

Resets direct:
- Local storage read-error
- Master check
- Early check
- ROS addr check

SYSTEM RESET A AT P2 DEL

Resets direct:
- MS compare
- Halt state
- Wait latch
- ASC II latch
- Skew data latches
- Skew select bits 0-7

Sets direct:
- Skew select bit P
- Enable latch
- External interrupt bits 2-7

SYSTEM RESET

Resets direct:
- Op out Mpx
- Repeat ROS address latch
- Stop clock latch

Sets:
- ROAR address 005
- Write latch if MS read cycle
- CPU tag reg bit P
- SPLS reg bit P
- A0 reg parity
- A1 reg parity
- YA stat parity

RESET CHAN NOT MS READ

Forces

CHAN SYSTEM RESET AT P2 DEL

which forces

CHAN SYSTEM RESET

which resets
- Early RTPT
- ADR-1 to ROSCAR

and sets
- Select in latch
- SC1 and SC2 tag reg P bit
- and allows gated T clock

CHAN System Reset

forces

CHAN System Reset at P2 Del

which resets
- SC1 and SC2 tag reg

Chan System Reset

forces

Clear SC1 Errors which resets
- IF control check
- Chan control check
- Tag check
- Buffer data check
- Bus-in parity error latch
- W0 parity error latch

Chan System Reset

forces

+Clear Chan SC1

which resets:
- Chan flag reg bits 0-5
- SC1 interrupt request
- SC1 W buffer
- Data operation latch

Chan System Reset

forces

Clear Chan at P2 Del

which resets:
- T0, T1 reg

Chan System Reset

forces

Clear Chan SC1

which resets:
- Waiting for IF response latch
- Select SC1 ROSCAR latch
- Load mode
- 1401-1410 mode
- Tape odd parity
- Disk load mode
- PSA SC1 latch
- Prog check SC1
- ROSCAR interlock
- Unit unavailable SC1
- Unit select latch
- Suppress out to SC2 latch
- Suppress out latch
- Address out
- Inhibit select out
- WLR latch
- Chaining check latch
- Start latch

Sets:
- Chan, flag reg P bit
- T0,T1, P bits

NOTE: Above resets and sets are developed for SC2 in an identical manner.

SYSTEM RESET LATCH

Resets:
- Log 1 latch
- Prevents T clock reset of ROS addr comp latch
- Prevents set of read MS latch by read MS control during T time.

SYSTEM RESET STOP T CLOCK

- Sets stop clock latch
- Allows latch back of manual store display latch

Figure 30. Hardware System Reset Timing Chart, Sheet 2 of 2

6. All latched machine conditions are reset (ISA, PSA, YCI, YCD, etc.).

7. Error stat Y12 is set on.

8. The enable latch is set.

NOTE: This latch, together with stat Y12, forces a hardstop following any error detected in the following CPU checkout microprogram.

9. A clear-channel operation is forced and channel interfaces are reset. This resets all latches controlled by the channels and gives each control unit attached a general reset.

10. The ROS address 005 is forced (Figure 23). This is the first microinstruction of the CPU checkout routine (CQ5111).

CPU selector channel checkout is executed as described in "CPU Checkout Programs."

Any errors detected cause a hardstop as a result of setting enable and Y12. After CPU checkout is complete, the microprogram branches to the system-reset microprogram routine.

Microprogram System Reset:

1. Entered after CPU and channel check-out.

2. System in disable mode during validating of local storage locations.

3. Channels selectively reset after log out.

4. Main storage validated only if system reset is entered by pressing load pushbutton.

5. Exit from system reset depends on how CPU-channel check-out has been entered.

The system reset microprogram is always entered on completion of the CPU and channel check-out microprogram. The CPU and channel check-out microprogram can be entered for five distinct reasons. Different stats or latches are set on entry to the microprogram system reset, indicating why system reset is entered.

CPU check-out test initiated on the console: Y3 is on.
After log out: Y7 is on.
After pressing the system-reset pushbutton: the halt latch is on.
After pressing power-on pushbutton: the halt latch is on.
After pressing load pushbutton: the load stat is on.

Figure 27 is a general flow chart of the system-reset microprogram.

The machine is in disable mode when the microprogram is entered; the general purpose registers, floating-point registers and the PSW area in local store are validated (read out and written back with good parity). The dump area in local store is set to read-out state (blanks). At this stage, the system is set to enable state.

If system reset is entered after log out (Y7 on), the stats Y4, Y5 and Y6 have been set during the log out routine to signify which channel has been logged out and as a result must be reset now.

A test is then made on the load stat (Y15) and, if it is on, the complete main storage is validated.

As seen on the microprogram data flow, four paths could be taken at the end of microprogram system reset:

1. Go to stop loop if the halt latch is on (after power-on or system-reset pushbutton is pressed).

2. Go to the initial program load (IPL) routine if the load stat (Y15) is set (after pressing the load pushbutton).

3. Go to the machine check interrupt routine if Y7 is on or none of the tested stats are on (after a log out). (Later, you will see that this path is also taken when performing loop on MS or loop on ROS.)

4. Go back to the CPU check-out routine if Y3 is on (diagnostic-control switch on CPU position and the start pushbutton pressed).

PSW Restart Pushbutton

- **Loads PSW from main storage location zero into local storage.**
- **Machine must be in a stopped state.**
- **Provides a means of restarting a program loaded with load pushbutton.**

The PSW restart pushbutton forces ROAR to 407 (hex) — CAS QC111 — and from here a functional branch to 4CA (hex) is made. The IPL microprogram is entered at the point where the PSW from main storage location 0 is loaded into local store.

You must first press the stop or system-reset pushbutton to set the system into the stopped state before the PSW restart pushbutton is active.

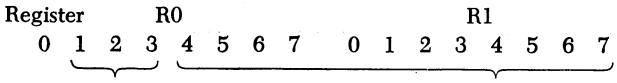
Storage Select Rotary Switch

- **This switch is used with the display and store pushbuttons to display or store areas accessible by the program.**
- **Display and store pushbuttons are active only in the stopped state (stop loop).**
- **Pressing the store or display pushbutton starts microprogram that always terminates in the stop loop (see the microprogram data flow, *System/360 Model 40 Comprehensive Introduction, Field Engineering Manual of Instruction*, Form 223-2840).**
- **Machine error results in a hardstop.**

The storage-select rotary switch allows display or store operations into main storage, storage protect, local storage and these local storage areas where program information is held: general-purpose registers, floating-point registers, and PSW. The instruction counter in the PSW can be directly stored or displayed on

the IC position. The display pushbutton forces address 402 hex into ROAR if the system is in the stopped state (stop loop). The store pushbutton forces address 403 hex into ROAR if the system is in the stopped state (see Figure 23).

The display (store) microprogram routine encodes the storage select switch setting (CAS QC081) as:



STORAGE SELECT ROTARY SWITCH ENCODING	VALUE INTO R0 REGISTER BIT POSITIONS		
	1	2	3
SP	0	0	0
IC	0	0	1
GP	0	1	0
FP	0	1	1
MS	1	0	0
PSW	1	0	1

This encoding allows the microprogram to take different branches for different storage-select positions.

The binary address keys and the binary data keys (console panel F) are used with the storage-select rotary switch.

SP (Storage Protect)

Display: The A register is set by storage address keys and is used to read main storage. Storage data lights; byte 0 is blank; byte 1, bits 0-3, has the SPLS data register which has just been set from SPLS location readout; byte 1, bits 4-7, has PSW key taken from LS 44, hex.

Store: The A register is set by storage address keys and is used to read main storage. Storage data lights; byte 0 is blank; byte 1, bits 0-3, has the SPLS data register which has just been set from storage data keys (byte 1, bits 0-3); byte 1, bits 4-7, has the PSW key taken from LS 44 hex. New SPLS data register contents are written into SPLS addressed by address keys.

IC (Instruction Count)

Display: Storage address lights, byte x has compressed byte taken from byte 1 of LS 46 hex which is the high-order IC. Storage address lights, bytes 0 and 1 have the two low-order bytes of IC taken from LS 47 hex. Storage data lights: byte 0 has ILC, CC, and program mask taken from LS 46, hex byte 0; byte 1 has IC high-order byte uncompressed taken from LS 46, hex, byte 1.

Store: Storage address lights have storage address keys. A0 and A1 are written into LS 47 hex. Storage data lights: byte 0 has ILC, CC, and program mask taken from LS 46, hex, byte 0; byte 1 has Ax register, D0 and D1 are written into LS 46 hex.

MS (Main Storage)

Display: The A register is set by storage address keys and is used to read main storage. The D register has main storage data readout which is written back into main storage. Display is in storage data lights.

Store: The A register is set by storage address keys and is used to read main storage. The D register is set by storage address keys and is written back into main storage.

NOTE: When the addressed location is not available (ISA), the store operation is changed to display operation.

PSW (Program Status Word)

Display: The A register is blank except for byte 1, bits 6 and 7, which have the storage address keys used to select the PSW halfword required. Storage data lights have a halfword of the PSW taken from LS 4x hex.

Store: The A register is as for display. The D register has the storage data keys and is written into the PSW in LS 4x hex, the halfword affected being selected by the storage address keys, byte 1, bits 6 and 7.

GP (General Purpose Registers)

Display: The A register is blank except for byte 1, bits 0-3 and bit 7, which have the register and halfword selected for display on the storage address keys. Storage data lights have the halfword of the register selected taken from LS.

Store: The A register is the same as it is for display. Storage data lights display the storage data keys which are written into LS at the position selected by the storage address keys.

FP (Floating Point Registers)

Display: The A register is blank except for byte 1 (bits 1 and 2, 6 and 7) which have the register and halfword selected for display in the storage address keys. Storage data lights have the halfword of the register selected taken from LS.

Store: The A register is the same as for display. Storage data lights display the storage data keys which are written into LS at the position selected by the storage address keys.

Address Compare Switch (Figure 22)

- **This switch allows the operator to stop, loop or repeat on a select ROS address, MS address or both.**
- **Test indicator is lit when switch is not in process position.**

Three sync points are available from circuits controlled by this switch. They are:

1. Sync MS latch – sync pulse generated when the

address on SAB equals the address key contents. 01A-D3H6-D13 (ALD KH142).

2. Sync ROS – sync pulse generated when the address on ROSAB equals the data key contents. 01A-D3H6-D12 (ALD KH142).

3. Sync ROS and MS – sync pulse generated when conditions 1 and 2 are both satisfied. 01A-D3H6-D10 (ALD KH142).

NOTE: These sync points are always active and are not dependent on the address compare switch setting. However, the ROS address compare latch is set by T clock pulses and is not active on hardware forced addresses when the T clock is stopped.

Stop on ROS

This switch forces hardstop on equal comparison of ROSAB, and the data keys. The microinstruction specified is not executed.

Hardstop does not occur on hardware-forced ROSAB addresses. However, when hardstop occurs, ROAR contains the address set in the data keys.

The ROS address compare latch causes the stop clock latch to be set when the contents of the data switches equal the address in ROSAB (Figures 23 and 31). As a result, the T clock stops at the end of the current machine cycle, prior to execution of the selected microinstruction.

Loop on ROS

Looping does not occur on hardware forced addresses. This switch may be used for looping to diagnose or scope intermittent machine errors. Looping on ROS is possible during an IPL routine if the load stat (Y15) is on (Figure 38).

On an equal comparison of the data key setting and ROAR contents:

1. Addressed microinstruction is executed.
2. Hardware system reset is forced.
3. CPU checkout is executed.
4. Microprogram system reset is executed.
5. Machine check interrupt is forced.

NOTE: The sequence listed above is not valid if the ROS address specified in the data keys is that of a microinstruction within CPU checkout or microprogram system reset. In this case, the machine check interrupt is not executed and the microprogram goes directly to the hardware system reset on the address equal condition.

The ROS address compare latch and system reset latch are set when ROSAB contents equal the data keys (Figure 23). The system reset latch forces a hardware system reset followed by a CPU checkout. A microprogram system reset is performed and exit made to the machine check interrupt microprogram. The machine check new PSW is loaded, and a branch to the address specified in the PSW takes place.

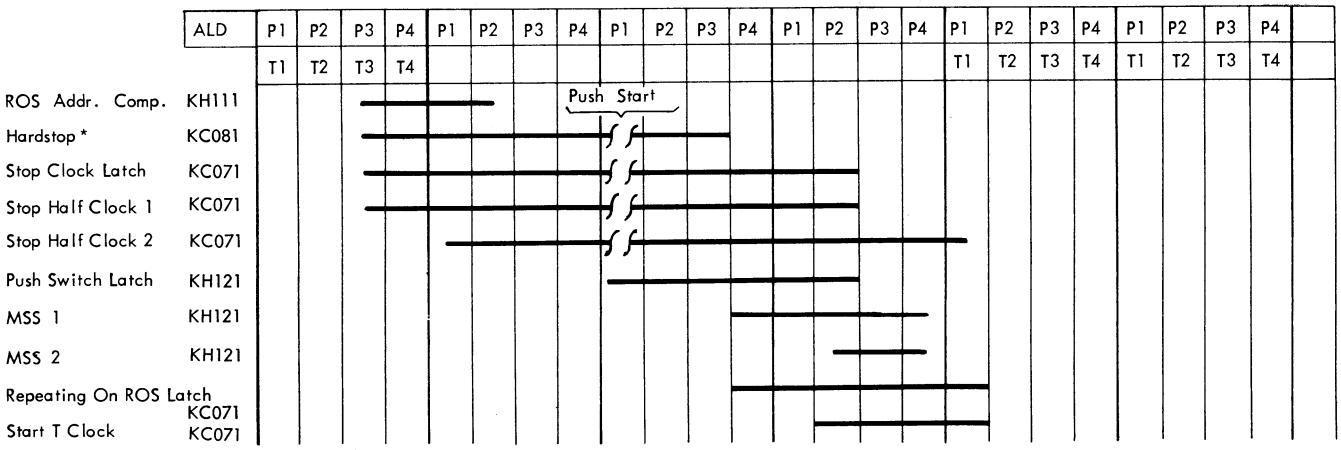
NOTE: Any error detected prior to address compare condition also causes a machine check interrupt. This means that the return point is the same regardless of machine errors encountered.

Repeat on ROS

Repeat on ROS causes repetitive execution of the microinstruction specified by the data keys (Figures 22, 31, and 32). It may be used in single cycle mode. *Repeating does not occur if the check control switch is set to stop.*

This feature may be used to diagnose or scope ROS data or address failures.

The address specified in the data switches is forced into ROAR and two P cycles taken in which the microinstruction is fetched by hardware. The T clock is then



* Prevents Machine Initiated Log Out

Figure 31. Stop on ROS Timing Chart

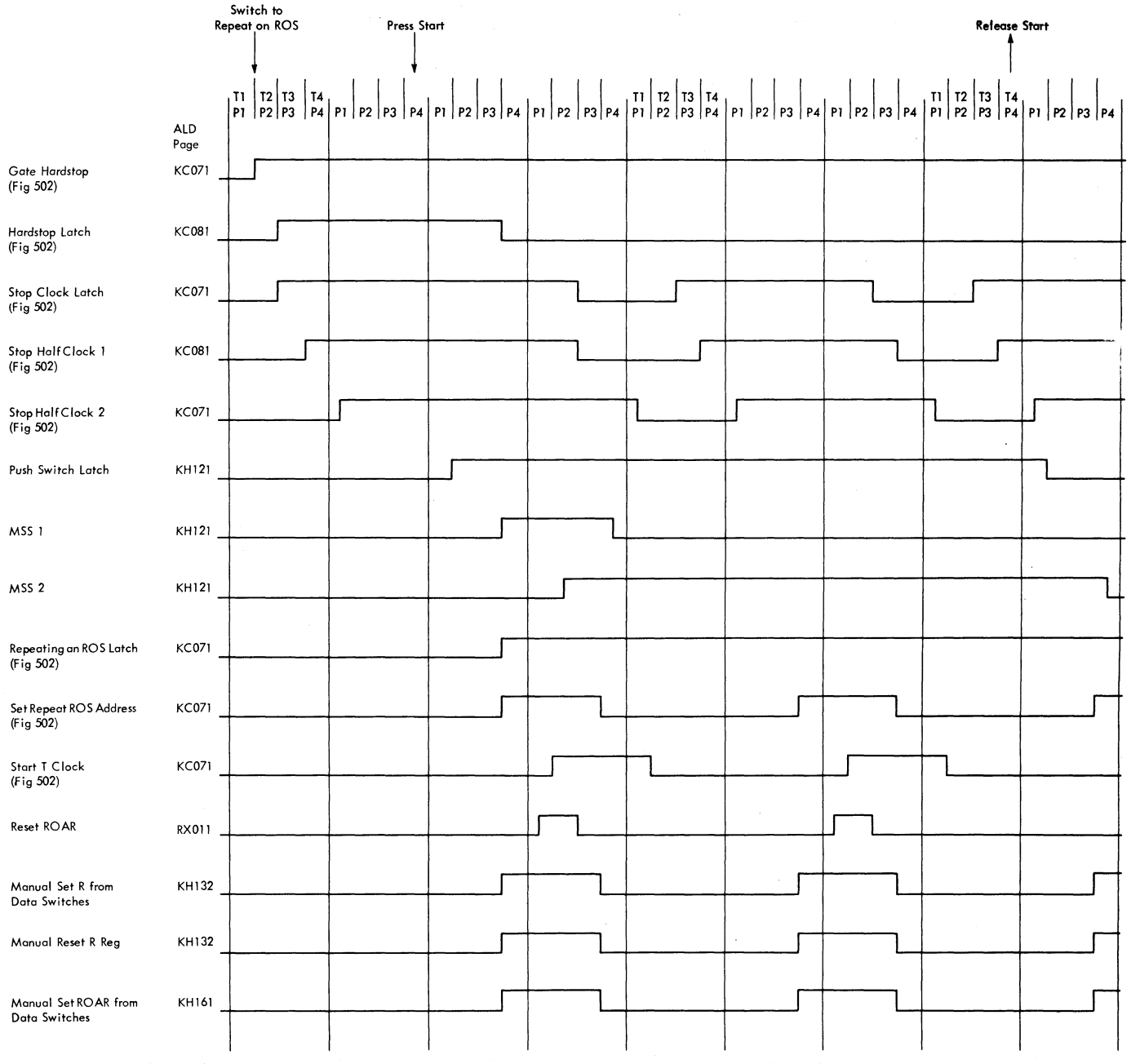


Figure 32. Repeat on ROS Timing Chart

started and the microinstruction executed. The T clock is stopped and the sequence is repeated. The machine is disabled unless the check control switch is set to stop.

Stop on MS

Stop on MS causes the manual stop loop to be entered following an equal comparison of the address on SAB and the address keys. The stop loop is entered after execution of the machine-language instruction in which the equal condition is detected.

Stop on MS is commonly used by the customer for program debugging.

The halt latch is set when main storage read is called following an equal comparison of the A register contents and the address keys (Figure 23). The halt latch causes a PRI branch in the next I-fetch routine. The stop loop will be entered following a timer update.

NOTE: This feature is effective only if these conditions are present:

1. Not Mpx I/O mode.

2. CPU addressing MS not UBA.
3. Read memory control.
4. Trap or storage address compare (SAC) is present.

Loop on MS

Loop on MS causes the following to occur on equal comparison of the A register contents and the address keys (see Figures 23 and 34).

1. Stop loop is entered after execution of the current machine-language instruction.
2. Hardware system reset is forced.
3. CPU checkout routine is executed.
4. Microprogram system reset is executed.
5. Machine check interrupt is forced.

Loop on MS may be used for looping to diagnose or scope intermittent machine errors.

The halt latch is set when the address on SAB is equal to the address in the address keys and MS read is called. The halt latch forces a PRI branch in the next I-fetch routine. The stop loop is entered and a hardware system reset is now forced. CPU checkout is executed followed by a microprogram system reset which exits to the machine check interrupt routine. The machine check new PSW is loaded, and a branch to the address specified in the PSW occurs.

NOTE: When looping on MS, machine errors may occur. In this case, a log out occurs and a machine check interrupt is forced. Thus, the restart point will be identical regardless of the cause. Realize that the machine language instruction under test may be altered or destroyed, depending on the type of error encountered. Thus, take care when using this switch position, that the error condition is not one that will alter MS data (e.g., D register parity checks).

Loop on MS and ROS

Loop on MS and ROS loops on equal comparison of the A register contents and the address keys, followed by an equal compare of ROS contents and data keys.

After both equal conditions exist:

1. The addressed microinstruction is executed.
2. Hardware system reset is forced.
3. CPU checkout is executed.
4. Microprogram system reset is executed.
5. Machine check interrupt is forced.

The halt latch is set when the contents of the A register equal the address keys and the contents of ROSAB equal the data keys (see Figure 23). CPU checkout is executed, followed by a microprogram system reset which exits to machine check interrupt routine. The machine check new PSW is loaded, and a branch to the address specified in the PSW occurs.

NOTE: Refer to the note following "Loop on MS" for conditions of use.

Stop on MS and ROS

Stop on MS and ROS is used to stop on a specified ROS address within a particular machine language instruction. It forces a hardstop after equal comparison of the A register contents and the address keys; and ROSAB contents with the data keys.

The microinstruction specified is not executed.

Hardstop does not occur on hardware-forced ROAR addresses.

The MS address compare latch is set on an equal comparison of the A register contents and the address keys (see Figure 23). The ROS address compare latch is set on an equal comparison of ROSAB and the data keys. The two latches then cause the stop clock latch to be set, which stops the T clock at the end of the current machine cycle, prior to execution of the specified microinstruction.

Rate Switch

The rate switch controls the extent of machine operations for each depression of the start pushbutton.

The test lamp is lit when the switch is not in the process position.

This switch executes one machine language instruction, microinstruction, or hardware cycle for each depression of the start pushbutton. The rate switch provides stepping machine instructions in the instruction step mode and stepping microinstructions in single cycle mode.

PROCESS Position

The PROCESS position is only active if the system is in the stopped state (manual indicator on):

1. Address 400 hex is forced into ROAR (diagnostic control off).
2. The halt latch is reset.
3. Microprogram loads PSW from local store into data flow.
4. Wait loop is entered if bit 14 of the PSW is 1.
5. I-Fetch is entered if bit 14 of the PSW is 0.

For the over-all microprogram sequence, refer to the microprogram data flow in *System/360 Model 40 Comprehensive Introduction, Field Engineering Manual of Instruction,* Form 223-2840.

The start switch is active only if the system is in stopped state (Figure 23). In stopped state, the halt-state latch is on because the system is in the stop loop where the control Manual (CB = 6, CD = 3) is given. The MSS pulses are generated and ROAR is reset and forced to start address 400 hex. Note that the T clock is stopped for one cycle by turning on the stop-clock latch (Figure 502) with the conditions: manual set ROS address and not MSS 2 and P3 or P3 del. The inhibit-on-error latch also is turned on for one cycle (Figure 502) while forcing ROAR to address 400. The

halt latch is turned off when the start switch is activated. Refer to the timing chart (Figure 24) for start pushbutton sequence. Once the new address has been forced into ROAR and the T clock is started again, the microprogram (CAS Sheet QC071) proceeds by loading the PSW from local store into the data flow (Figure 26).

The wait loop would be entered if PSW bit 14 is one. Note also that the MI stat is re-evaluated depending on interrupt request latches and the system mask bits of the PSW. When I-fetch is entered, a test is made on the instruction address (IC) for validity, and the program check interrupt routine is entered if this address is not valid.

If the wait bit in the PSW is on and the machine enters the wait loop, the PRI condition is tested and, if present, the microprogram proceeds in handling the interrupt.

Instruction Step (INSN STEP) Position

This position sets halt latch and generates program interrupt (PRI).

The stop loop is entered every time an instruction is executed, and the PSW is always completely updated in local store. Any PRI condition generated by a source of higher priority than halt has its PSW loaded. The instruction step position allows one complete machine language instruction to be executed for each depression of the start pushbutton, followed by the first halfword I-fetch of the next instruction. It is commonly used for program debugging and machine-failure analysis.

Pressing the start key results in loading the PSW from local store into the data flow (see "Press Start Pushbutton with Rate Rotary Switch in Process Position"). Remember that PRI is tested during every I-fetch.

The PRI condition is ignored on the first cycle after depressing the start pushbutton (the microprogram turns Y6 on). This means that PRI is detected only after the complete instruction is executed and during I-fetch of the next instruction. The microprogram takes the PRI branch, updates the PSW in local store, and enters the stop loop via the microprogram display routine. (See microprogram data flow in *System/360 Model 40 Comprehensive Introduction, Field Engineering Manual of Instruction*, Form 223-2840.

If, when the PRI branch is taken and the microprogram tests to find which source generated PRI, it finds a source of higher priority (I/O interrupt, for example), the higher priority interrupt is taken. This means that the current PSW is stored in an old PSW main storage location and the corresponding new PSW is loaded into local store and PRI is tested again. PRI is present because instruction step mode sets the halt latch during TRAP test, and the system enters the stop loop. Pressing the start pushbutton again now results in execution of the first instruction from the interrupt program under control of the new PSW.

SINGLE CYCLE Position

The single cycle mode generates hardstop condition.

Pressing start switch generates MSS pulses.

The stop-clock latch is allowed to turn off and one T cycle is taken. Hardware cycles (log out, dump cycle, etc.) are always taken.

A main storage read or write order given in a T cycle is completed.

Setting the rate rotary switch to SINGLE CYCLE generates the gate-hardstop condition (Figure 502). This condition, with the repeating-on-ROS latch off, sets the hardstop latch at P3 time. The hardstop condition keeps the stop-clock latch on, and the stop-half-clock 1, and stop-half-clock 2 are active. Pressing the start switch generates the MSS1-MSS2 pulses (Figure 18) and the repeating-on-ROS latch comes on. This latch gives the start-T-clock condition and resets the hardstop latch. The stop clock, stop-half-clock 1 and stop-half-clock 2 conditions are inactive for a short time to allow one T cycle. See Figure 33.

Note that the ROS address normally generated by hardware when the start pushbutton is pressed is not generated if the system is not in the stop loop (halt state latch on). See Figure 23.

Whenever hardware cycles are to be executed (hardware log out, dump or undump cycle, hardware system reset, trap hardware cycle), they are always executed and cannot be stopped in single cycle because they do not require T time. When a main storage read is executed in this mode, the T clock stops at the end of the cycle, but the main storage cycle is completed and data is transferred into the D register. Similarly, when main storage write is executed, the main storage cycle is completed and data from the D register is transferred into main storage.

For each depression of the start pushbutton, the processor advances by the minimum number of clock cycles possible, returning after each advance to the hardstop state (Figure 33). I/O instructions can be single-cycle advanced to the point where data transfer operation begins. When the start pushbutton is pressed at this point, data transfer operation begins and runs to completion. Should an interrupt occur, it may be single cycled.

Check Control Switch

This switch controls machine actions in the event of an error. The test lamp is lit when the switch is not in the process position.

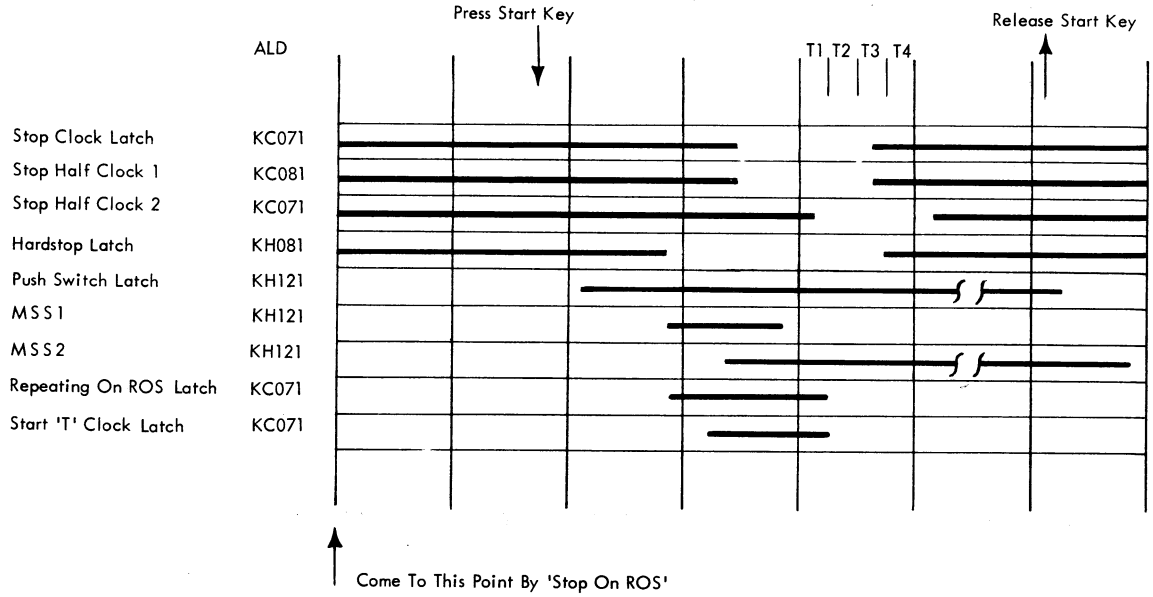


Figure 33. Start in Single Cycle Mode Timing Chart

Process

1. Place switch in normal position.
2. During execution of a machine-language program, a log out occurs (if enabled) following detection of a machine error.

Stop

1. Hardstop is forced following detection of an error.
2. It has the same effect on the machine as Y12 or Y15 being on.
3. Log outs are disabled in this position.

An error stop condition is generated when the check control switch is in the stop position. The error stop condition forces a hardstop on machine errors; or on the microcommands LOG or ICC. The setting of the enable latch has no effect when the switch is in the stop position (i.e., it is not possible to disable errors)

Check Restart

These actions take place when an error is detected:

1. The error latches corresponding to the failure are set.
2. Hardware system reset takes place.
3. CPU checkout is executed.
4. Microprogram system reset takes place.
5. Machine check interrupt is forced.

NOTE: The above sequence is not valid if the error is an intermittent failure, that is, detected within CPU checkout or microprogram system reset. In this case, the machine check interrupt does not occur, but the microprogram goes directly to the hardware system reset again. This means, in the case of an intermittent error in these two microprograms, that this switch position cannot ensure a consistent return path.

When an error is detected with check restart selected, the system reset latch is forced on and the normal machine check interrupt sequence is executed. The new machine-check PSW is loaded and a branch effected to the location as specified by the instruction address in the PSW.

Refer to "Check Restart on IPL."

Disable

Disable prevents hardstop or log out following detection of an error. Errors light their corresponding indicators but machine operation continues.

Over-all check latches (early, late, control) remain set but the individual checks may be reset.

Console Panel H

Power-On Pushbutton

- **Depressing the power-on pushbutton initiates system power on.**
- **The power-on pushbutton is lit after sequencing on and receiving power good from all I/O devices on line.**
- **Power-on sequence results in entry to the manual stop loop following a hardware and microprogram system reset.**

The system power-on sequence is described in "Power Supplies," *System/360 Power Supplies and Appendices, Field Engineering Manual of Instruction,* Form 223-2845. As long as the power good relay is not picked, the power-not-good signal permanently resets the power good latch (Figure 28). During this time, the halt latch, system-reset latch, and stop-clock latch are

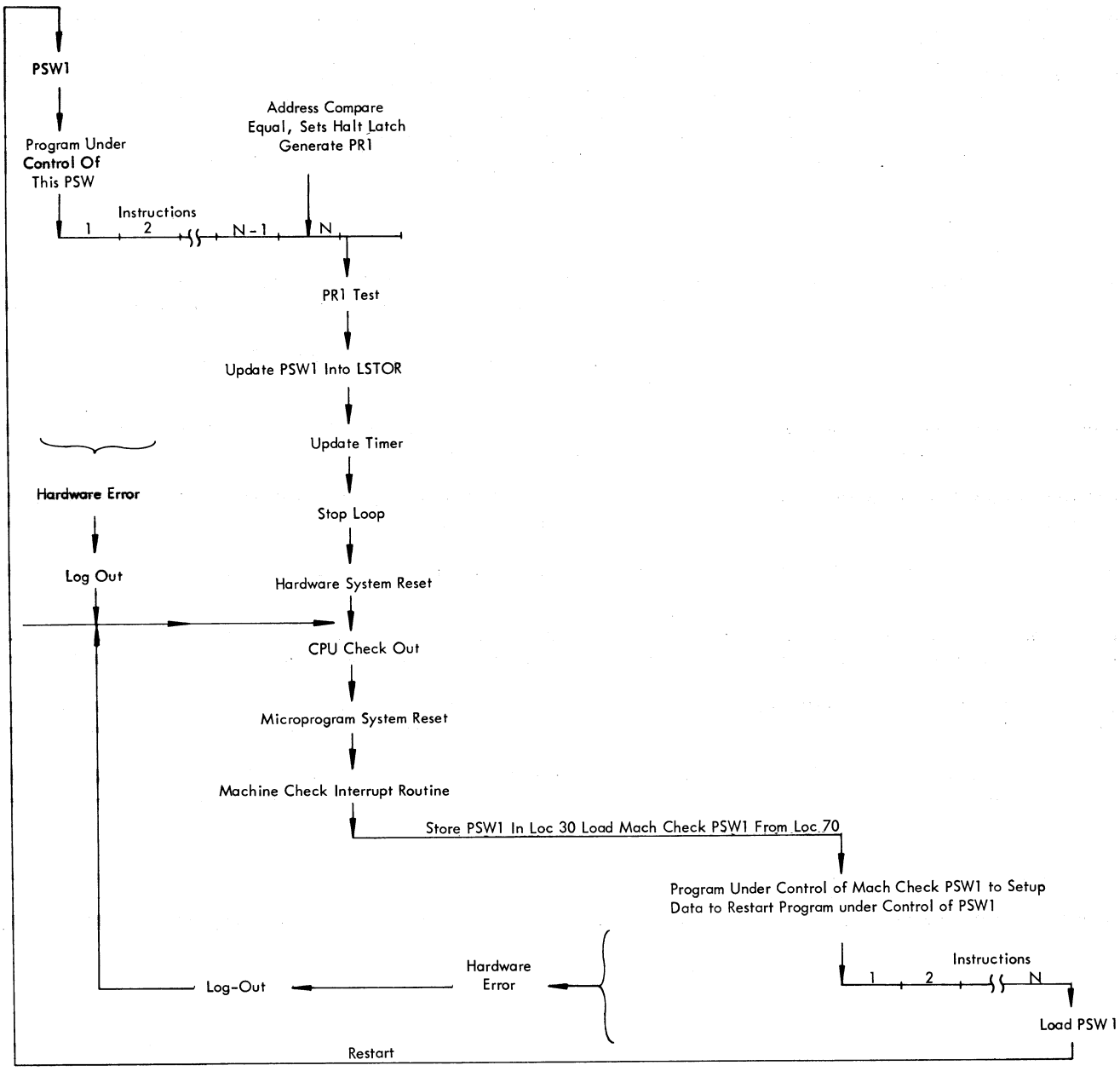


Figure 34. Loop on Main Storage

forced on. T pulses are not available as long as the power-good latch is not set. The power-on-reset line to main storage resets main storage circuitry, while the system reset latch resets logic within the system.

As soon as the power-good relay picks, the stop-clock latch can be reset (the line system reset stop T clock is inactive after 6 microseconds (Figure 502). When the start-T-clock latch is on (reset on), the reset of the stop-clock latch occurs at P3, and T time is now available. The system-reset latch is reset at T1, and the CPU and channel check-out microprogram is entered. After a successful checkout, the microprogram system reset is entered and the machine enters the stop loop (halt latch is set on by power not good). In the stop loop, the manual indicator on the console is on. The halt-state latch is set by the microprogram order, Manual, given in the stop loop; the manual indicator is connected to this latch. Normally, the customer loads his program and resets the halt latch by pressing the load pushbutton. Any machine errors during the power on sequence result in a hardstop.

Power-Off Pushbutton

Pressing the power-off pushbutton initiates a normal power-off sequence.

Power is not removed from K1 or the 24v power supply.

Load Unit Switches

Load unit switches are set to give the address of the I/O unit used to load the program.

The channel address is set into the IPL microprogram from the left load unit switch via the R register byte 0, bits 5, 6, 7.

The center and right load unit switches provide the control unit and device address for the IPL program via the R register byte 1.

Interrupt Pushbutton (Figure 18)

Pressing the interrupt pushbutton causes an external interrupt request to be generated if the external mask latch is on. This pushbutton is not effective in the manual stop loop.

This pushbutton is explained under "External Interrupts" in the *IBM System/360 Model 40 Theory of Operation, Field Engineering Manual of Instruction,* 223-2844.

Load Pushbutton

- **The load pushbutton is active only when in the stop loop.**
- **Set Y15 to control the load operation, and force a hardstop on errors.**
- **Forces a hardware system reset, CPU and selector channel checkout, a microprogram system reset, and a main storage validate; followed by by a branch to the initial program load (IPL) microprogram (QC121).**

The IPL microprogram routine sets up an initial CCW and selects the unit addressed by the load-unit switches. The initial CCW allows one PSW and two additional CCW's to read in. The microprogram waits in the IPL wait loop (CAS QC121, 4F6) until the I/O operation is completed. After completion of the I/O operation, the PSW read into location 0 becomes the current PSW. Any error occurring before the machine starts executing the program specified in the first PSW results in a hardstop or hang-up.

To load a program, the channel and I/O unit number of the I/O device must be set into the load unit switches. When the load pushbutton is pressed, the load stat (Y15) and the system-reset latch are forced on (the halt latch is reset). As a result, the hardware system reset is performed, followed by the CPU and channel check-out and the microprogram system reset. Main storage is validated during the microprogram system reset (see "System Reset"). At the end of the microprogram system reset, the load stat is successfully tested (CAS QC121) and the IPL microprogram routine is entered.

An initial CCW is assembled by microprogram, starting at main storage location 0 and having the following hex value: 0200, 0000, 60XX, 0018. This command code means read into data address 0. The count 18 hex signifies that 24 bytes are read in with this CCW. These 24 bytes are 8 bytes for a PSW and 16 bytes for two CCW's. The assembled CCW in location 0 also has the command-chaining and the suppress-incorrect-length flags on.

Automatically after the PSW and the two CCW's are read in, command chaining from the assembled CCW to the first CCW read into main storage location 8 is obtained. Note that the assembled CCW in location 0 is overwritten by a PSW. After the second CCW, further activity is up to the program; chaining could be programmed to following CCW's and so on. The program, however, does not start before the chain of CCW's initiated by IPL is completed. Between fetching CCW's, the microprogram loops in the IPL wait loop (CAS QC121). In this loop, data service for the selected channel is obtained by microprogram interrupts (dumps for the multiplex channel and buffer service break ins for a selector channel. When a CCW no longer specifies chaining, the microprogram branches out of the IPL wait loop, assembles the CSW, and goes into the load PSW routine. In this load PSW routine, the PSW read in main storage location 0 is set into the data flow (current PSW), and program execution starts at the address specified by IC. During the load PSW routine, Y15 is reset and any further machine error (machine enabled) results in a log out. Note that during the IPL routine, a microprogram hang-up can occur in different places.

System Status Indicators

System Indicator:

1. Indicates one of the usage meters in console panel G is running.
2. Lights when one of these conditions exists:
   a. System is not in wait, stop or hardstop state.
   b. Any attached I/O device or control unit is operating.

Manual Indicator: MANUAL indicates that the system is in the stop loop. This state is entered when the stop pushbutton or the system reset pushbutton is depressed.

Wait Indicator:

1. Indicates that the wait bit in the current PSW is a binary one.
2. Instruction count is displayed in the IC or storage address lights.

Test Indicator: Any one of the conditions listed below will cause the test indicator to glow:

Rate switch not set to process.
ROBAR display key not set to ROBAR.
Diagnostic control switch not set to the off position.
Address compare switch not set to process.
Channel test switch set to manual.
Reverse data parity key on.
Multiplex store key on.
Disable interrupt key on.
Disable interval timer key on.
Manual interface keys on.
Check control switch not set to process.
Meter switch set to the CE position.

The lamp test key will not cause the test indicator to light.

Load Indicator: Is identical to Y15.

Console Operations (Storing and Displaying Procedures)

Procedures for storing or displaying information are shown in Figures 35, 36, and 37.

Checkout Programs

CPU and Selector Channel

The microinstructions in this program are grouped into sections each consisting of one, two, three or five microinstructions.

Each section sets up and tests certain machine conditions after exercising the various data paths, registers and stats.

A branch into one of twelve microinstructions is taken at the end of each section. A branch into words 0EC, 0EF, 07D, 07E or 53D indicates that a program error has occurred in some previous group. A branch into words 00E, 0EE, 07C, 07F, 13C and 13F causes a functional

Storage Select Switch Position	Display Operation	Store Operation
SP (Storage Protect)	Set address in address keys Press display pushbutton SP data register in data lights byte 1 bits 0-3 PSW key in data lights byte 1 bits 4-7	Set address in address keys Set data keys byte 1 bits 0-3 to new SP data Press store pushbutton PSW key will not be altered in this position, see PSW position
IC (Instruction Count)	Press display pushbutton IC contents in address lights IC byte X expanded in data lights byte 1 Program mask and CC in data lights byte 0 Note 4	Set new IC in address keys Press store pushbutton Program mask and CC will not be altered in this position. See PSW position. Note 4
MS (Main Storage)	Set address in address keys Press display pushbutton Data in data lights	Set address in address keys Set data in data keys Press store pushbutton Note 3
PSW (Program Status Word)	Set halfword in address key byte 1 bits 6-7 -- Note 2 Press display pushbutton Data in data lights Note 4	Set halfword in address keys byte 1 bits 6-7 -- Note 2 Set new data in data keys Press store pushbutton Note 4
GP or FP (General Purpose or Floating-Point Registers)	Register number in address key byte 1 bits 0-3 Halfword in bits 6-7 -- Note 2 Note: FP register numbers 0, 2, 4, 6 only Press display pushbutton Data in data lights Note 4	Register number in address key byte 1 bits 0-3 Halfword in bits 6-7 byte 1 -- Note 2 Set new data keys Press store pushbutton Note 4

MPX STORE (TOGGLE in ON)

NOT MS

Note 1: Manual stop loop may be entered in four ways:
1. Power on
2. Press stop pushbutton
3. Manually set ROAR to the address of the stop loop 469.
4. System reset

Note 2: Refer to panel F of console for halfword selection chart.
Note 3: Following the store operation, the address and new data will be displayed in the lights on panel F.
Note 4: Following this operation, the LS address will be displayed in panel D.

Figure 35. Displaying and Storing Procedure When in Manual Stop Loop

	Enter Data into Data Keys	Enter Data into Address Keys	Enter Address into Data Keys	Enter Address into into Address Keys		Setting of LSA Bus Display and Store Switch	Store Toggle Switch Setting	Mpx STOR key	Store/Display Roller Switch Position	Roller Toggle Switch to STORE
A Register	X								2	X
B Register	X								3	X
C Register	X								4	X
D Register	X								5	X
R Register	X								1	X
Local Storage	X			X					1	X
LSAR		X				LSAR	LSA			
H Register		X				H	LSA			
J Register		X				J	LSA			
Y Stats *	X						STATS			
Main Storage Data	X			X					7	X
Mpx Storage	X			X				X	7	X
ROAR			X						6	X

* Y 14 (IZT/IDQ) cannot be stored manually

Figure 36. Storing Procedure When in Hardstop Condition

branch to the beginning of the next sequential group.

In this way, the CPU check-out program exercises the data flow in small sections and tests that the machine is working up to this point before attempting to exercise another part of the data flow.

Since the error stat is set prior to starting the program, any machine check latch causes the program to hardstop on the step in which the error occurred.

NOTE: During the CPU check-out test, the red error-indicator lights come on. *No action should be taken* by the customer engineer because part of the check-out program is designed to force errors when the machine is in the disable state. If a genuine error occurs during the test, the machine will stop.

After the CPU itself has been checked, the program exercises the selector channels. Both selector channels are exercised one after the other except after a log out where only the channel that caused an error is checked.

Program Start

There are six ways of entering the program:

1. Depressing the system reset key.
2. Depressing the load key.

In both these cases the program is used to verify that most functions of the CPU are working.

3. Depressing the start key with the diagnostic switch set to CPU. Continuous program looping facilitates tracing intermittent CPU faults.
4. Immediately after an error log-out when the program is used to verify that the machine is returned to an operating state.
5. After a successful address compare in looping on ROS or MS.
6. After an error has occurred, with CPU check switch set to check restart.

Refer to Figure 38 for entries and exits from CPU check-out.

Program Starting Conditions: To define the start conditions, the YA and YB staticizers are set to different bit patterns depending on which keys have been depressed. The status of these is stored in local storage location 0 and used at the end of the program to identify the entry point. Settings for the four entry cases are:

1. The system reset key is depressed. A hardware cycle precedes the program during which:
   a. Registers A and D are reset.

To Display any addr
Store Disp in R addr

	Enter Address into Address Keys	Enter Address into Data Keys	Store/Display Switch Position	Display Roller Switch Position	Channel Display Switch Position	Channel Select Switch Position	Setting of LSA Bus Display and STORE	Mpx Stor Toggle Switch Down	Roller Toggle Switch on Display	Display Toggle Switch Setting	Must be displayed first or is wiped out	Roller Toggle Switch on Display will wipe out this reading
R Register *			1								X	X
Local Storage **	X		1						X			
A Register			2									
B Register			3									
C Register			4									
D Register			5									
ROAR			6						X			
Main Stor Data	X		7									X
ALU Ex, P, Q			Not 1	1								
Mpx Checks & IF			Not 1	2		Mpx						
IF Controls			Not 1	3		ROTATE						
Channel Controls			Not 1	4		SC1 / SC2						
Ext Interrupts			Not 1	6					X			
SP Data & Reg			~~Not 1~~ 7	7					X	Display Twice		
Direct Control			Not 1	8					X			
ROSAB										ROSAB		
ROBAR ***										ROBAR	X	
LSAR							LSAR				X	
H Register							H					
J Register							J					
Mpx Storage	X		7					X	X			
TO-T1			Not 1	5	TO / T1	SC1 / SC2						
W0-W1			Not 1	5	W0 / W1	SC1 / SC2						
W2			Not 1	5	W2	SC1 / SC2						
W3-W4			Not 1	5	W3 / W4	SC1 / SC2						
S Register			2			SC1 / SC2						
ROSCAR						SC1 / SC2				ROAR / ROSCAR		
SP Key ****			Not 1	5	W2	SC1 / SC2						
ROAR						Mpx				ROAR / ROSCAR		
SC Checks & IF			Not 1	4		SC1 / SC2						
W Buffer Flags												

*If the store display roller switch was on position 1 before stopping, the actual content of R register will be displayed. In every other position, the content of the R register will be destroyed.

**(The content of LSAR will be changed).

***The content of ROBAR will be destroyed if ROBAR display toggle switch is set out of position ROBAR.

****To display the storage protect key corresponding to a particular area of main storage or to a particular UCW, display one position of this area first. (Refer to "Main Storage Data" or "Multiplex Storage" above.) After setting the above conditions, this key will appear in the SP data register positions.

NOTE: The P bit appearing on this position of the lower roll chart is the result of exclusive ORing (not SPLS data parity, and SP key parity.)

Figure 37. Displaying Procedure When in Hardstop Condition

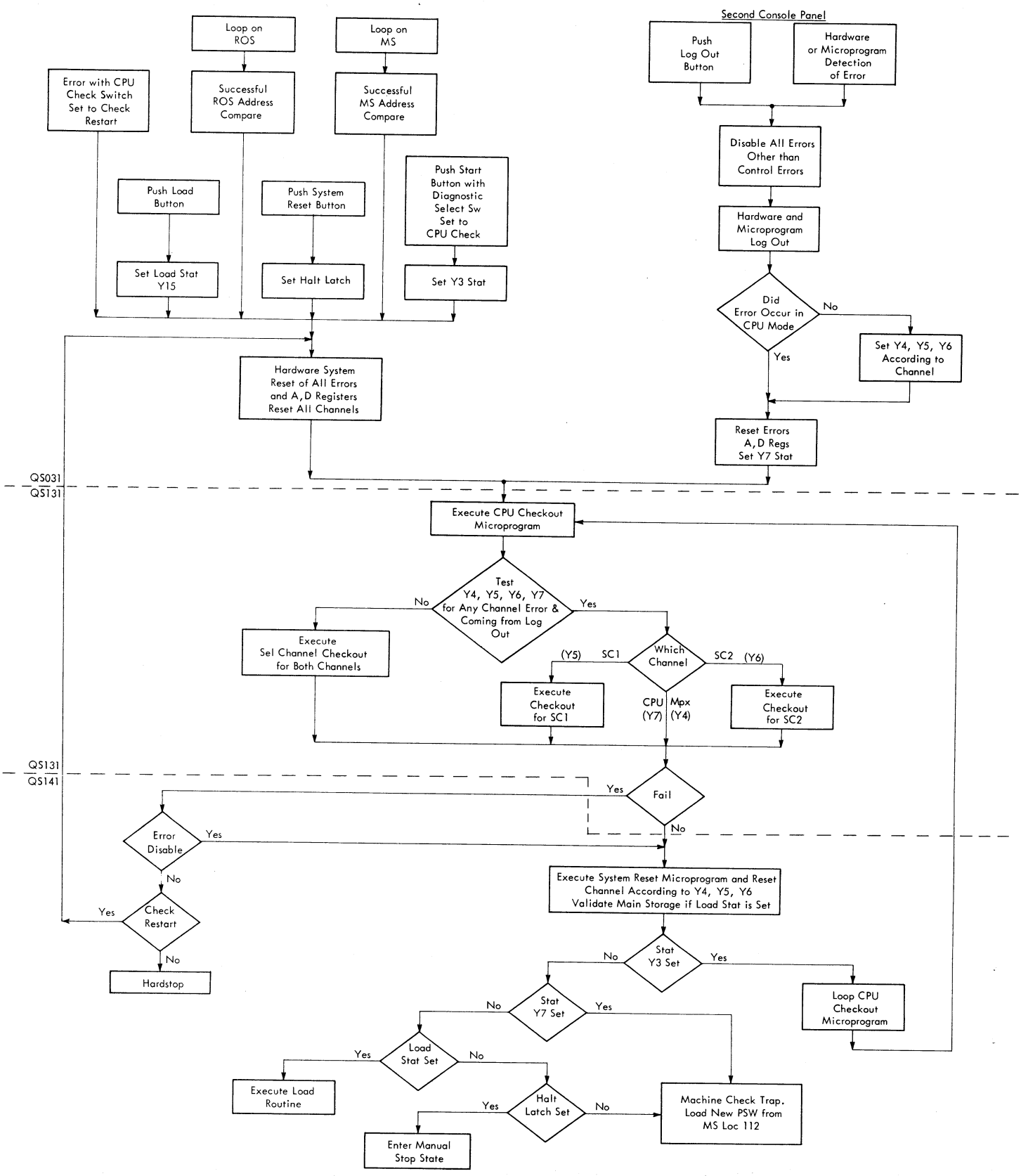


Figure 38. Entries to and Exits from the CPU Checkout Microprogram

b. All staticizers (including I/O) are reset, except the error stat, which is set.
c. All errors are reset.
d. The hold latch and external interrupts are reset.
e. Storage protect (including tag and data) is reset.
f. All latched machine conditions are reset.
g. Clear channel is forced.
h. Read only store address 005 hex is forced.
i. The program is set in error enable mode, unless the CPU check status switch is set to disable.

2. The load key is depressed.
The same hardware cycle occurs as in (1) except that in (b) both error and load stats are set.

3. Diagnostic control is set to CPU and the start key is depressed. Exactly the same sets and resets occur as in (1) except that in (b) Y0, Y3 and the error stat are set. Y3 is tested at the end of the program and, if it is on, the program will be reentered.

4. Error log out is completed.

The last few microinstructions of the log out routine reset the latches and registers until the status becomes:

a. The same as in (1).
b. The same as in (1) except that Y4-Y7 define the type of log performed. Y7 is on, and Y4-Y6 define which channels have been cleared. (Y5 = 0 if SC1 has been cleared, Y6 = 0 if SC2 has been cleared).
c. The same as in (1).
d. The same as in (1).
e. The log out routine branches out to read only storage address 005.
f. Enable mode is on.

Program Functions

1. Exercises the 18-bit data flow, with bit patterns entered from the emit field but including data generated in the H and J address registers.
2. Exercises the nine-bit data flow.
3. Checks the skew feature.
4. Checks the ALU functions (direct and indirect).
5. Reads and writes in one location of main storage.
6. Reads and writes in one location of Mpx storage.
7. Checks the increment function (up and down on H and J address registers).
8. Generates local store addresses from different sources and cross-checks with other means of generation.
9. Checks all machine conditions that are possible. Errors now cause a hardstop with the machine registers, latches, etc., unchanged.
10. Checks that stats can be turned on and off.
11. Checks read only storage addressing using two-way branches and 16-way function branches.
12. Exercises channel data flow: S register, T register, channel status, channel flags, W buffer.
13. Transfers the S Register to the main storage address bus (checking the contents of the location so addressed).
14. Checks channel microprogram branching conditions.
15. Checks reinterpret conditions.
16. Checks critical buffer timing.
17. Checks clear channel CL-CH micro-command.

Many of these tests are performed together in groups. Only a single failure is anticipated and consequently an error may be a result of more than one of these tests.

Program Limitations

1. Not all possible data patterns are used through the ALU, so that additional checks should be performed using all patterns. For example, the OR function is used, but not in all the combinations which guarantee the function.
2. ROS addressing is restricted to modules 0 and 5. Consequently, the top bits of ROAR are not set during the program execution.
3. Machine conditions are checked in the off state, but not in all possible on states. Thus, L4 is not checked in the on state for LSAR bit 4 on, others all off, LSAR bit 5 on, others all off, etc. This is also true of: L2 $\neq$ 0, ALU $\neq$ 0, and Q0 = 0.
4. Not all functions of the EX field are tested.
5. Only one main storage location and one multiplex storage location are accessed.
6. The following areas of the channel are not tested.
   a. Data flow associated with storage protect feature.
   b. ROSCAR (no channel activity).
   c. Transfers to and from interface (no channel activity).
   d. Flags byte bits CC, SKIP, SILI, R/W and Rd/Bkwd. (These are set by logic circuits during channel activity.)
   e. Status byte bits WLR, PROT, CDA, CC and CHAIN. (These are set by logic circuits during channel activity).
   f. Transfers from flags and status bytes to R bus. (This data flow is used only for display and log out; good parity on the transfer is not guaranteed).

Most of these additional facilities can be tested by conventional diagnostics. The advantage of the CPU check out program is that it checks a large part of the CPU logic circuits.

Documentation

The microprogram is documented on CLD sheets QS111, QS131, QS141, QS171, QS211 and QS221. It is also documented, in greater detail, on the machine status charts (MSC's). A machine status chart is available for each microinstruction executed in the program.

The data shown on the MSC is the data to be executed at the completion of each microinstruction when running in the single-cycle mode. The MSC also contains the CLD block for the microinstruction, together with descriptive notes giving the function of the microinstruction and possible failures of that function.

Checks

Two types of checks detected by the CPU check-out program are:

1. Hardware checks – a hardstop is forced with a check light on.
2. Program checks – the program takes a wrong branch and ends at one of the microinstructions containing stop: 0EC, 0EF, 07D, 07E, 53D or 53E.

Hardware Checks:

1. Inspect ROBAR.
2. Look up the machine status using ROBAR address to find MSC page (microprogram step number).
3. Study descriptive notes; if notes do not suggest the fault, it may be necessary to follow through the MAP's indicated in the descriptive notes.

Microprogram Check:

1. Neither ROBAR or ROAR give any indication to the failing section.
2. Compare the C, D, A, and B register states with the list given in the MSC (ECZ.00.001). This gives the last microinstruction executed and indicates the correct MSC page to be studied.
3. Compare expected register and latch states with console display.
4. Study descriptive notes; if notes do not suggest the fault it may be necessary to follow through the MAP's indicated in the descriptive notes.

Local Storage Pattern Diagnostic

This test, an internal microprogram diagnostic selected by the diagnostic control switch, exercises the local storage at machine speed with the worst-case data patterns. A flow chart of the diagnostic is shown in Figure 40. (See also Figure 912). The diagnostic pattern checks for the picking up or dropping out of bits in each location. Each location is subjected to a sequence of read, write, read, write, in consecutive machine cycles. The data written in the second write cycle is the complement of that written in the first write cycle. This tests if noise in the driver lines on selection is enough to switch the cores erroneously.

How to Operate

To operate the test, the diagnostic control switch is turned to LS pattern and the system reset key is depressed to bring the machine into the manual halt state. The start key is depressed and ROAR is forced to 00C (QS121) to initiate the test which consists of four routines.

Press system reset to exit from the test.

Description of Diagnostic

The complete test consists of four routines.

1. The worst-case data pattern is written into each storage location.
2. The complement worst-case pattern is written into each storage location.
3. The worst-case pattern for parity bits is written into each storage location.
4. The complement worst-case pattern for parity bits is written into each storage location.

Each routine consists of a write phase in disable mode (in which the pattern for this routine is set into the storage location) followed by a read-checking phase (in which the data is read out and checked for the expected result). If bits are dropped during the read-checking phase and even parity occurs in any byte of the R Register (checking occurs in the R Register), the machine stops in the hardstop condition. (Y12, the error stat, is forced on by hardware when the console keys are operated to start the test). If bits are dropped and odd parity still occurs, the machine stops with the microprogram check light on, as a result of microprogram detection of an unexpected result. Each phase is identical as far as microprogram is concerned. The initial conditions on entering each phase determine whether the machine is set into the disable state (write phase) or the enable state (read check phase).

In the write phase (disable) errors are ignored, while in the read checking phase (enable) errors force a hardstop or a microprogram check, depending on the number of bits that have been dropped or picked.

The microprogram is on CLD pages QS121 and QS181. Two loops are shown. Whenever a change of pattern is required to form worst-case conditions within the area under test, the microprogram branches into the other loop until a return to the original conditions is again required. Figure 40 shows the worst-case data patterns used in the areas.

Principle of Operation

Local storage is divided into areas as shown in Figure 39. The areas numbered 0 to F are those addressed by the first four bits of LSAR. Each area consists of 16 local-storage locations. Of these areas, those numbered 1, 5, 9 and D cannot be addressed.

Areas 8, A, and B can be addressed and are physically the same areas as C, E, and F. For this test, the areas that cannot be addressed are bypassed while those that can be addressed need only to be addressed once. Because of physical construction, areas 2, 6, and E require a different worst-case pattern from the remaining areas. The microprogram detects the area to be bypassed; the area requiring a change of worst-case pattern is the one after the bypassed area. The areas are checked sequentially; storage locations are addressed from the highest to the lowest within each area. For example, when area 3 is addressed, the test starts with the location address 3F in LSAR and works down the locations until address 30 is detected. The program moves to the next area and addresses location 4F.

Registers and Stats Utilization

The uses of the registers and staticizers in this test are as follows:

A register: Used in the formation of LSAR addresses for each area, or for the output from the location under test on the read-checking phase.

B register: B0 contains the data to control the pattern to be used for a particular area (one pass). It is set before entry into the pass for the 16 locations within the area and is effectively shifted one bit position left as each location is checked. (The high-order position is returned to the low-order position if a carry out of the high-order position occurs.) When the carry out occurs, i.e., the high-order position of B0 contains a one before the left shift, a change of pattern is required in the next location to obtain the worst-case conditions.

C register: Contains the master pattern being written into half the locations. C register content is compared with the expected A register result.

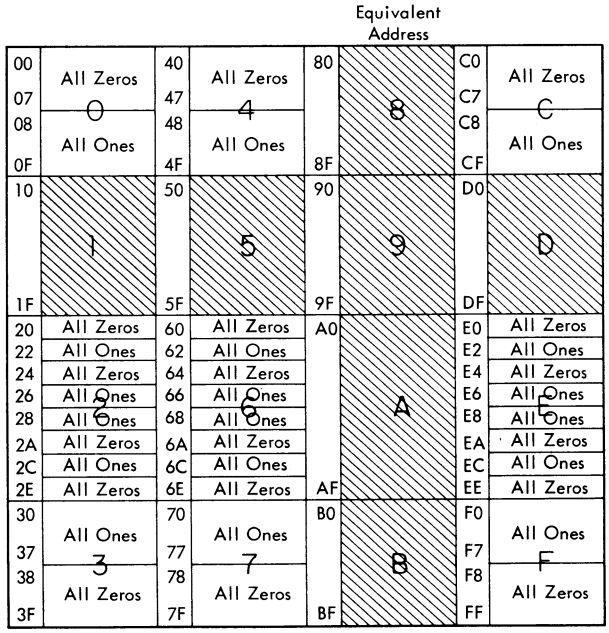
D register: Contains the inverse pattern read out from the location under the test during the second read operation of the read/write sequence.

H register: Used indirectly to address each location in turn. In conjunction with the L4 test condition, it determines when the area under test has been checked.

J register: Is used in conjunction with the L2≠0 and L4 test conditions to decide the area to be tested next and the pattern to be used to give worst-case conditions.

Staticizers:

Y0	= 0	Repeat mode.
Y0	= 1	Normal test operation.
Y1	= 0	Worst-case pattern test.
Y1	= 1	Address test.
Y2	= 0	Data bits test.
Y2	= 1	Parity bits test.
Y3	= 0	Normal operation.
Y3	= 1	Change the top two bits of the address on the next address update.



Note: Shaded areas do not physically exist.

Figure 39. Local Store Areas and Patterns Used in First Routine

Y4	= 0	Continue with the same pattern.
Y4	= 1	Change the pattern for worst-case conditions so set Y6 on.
Y5	= 0	Read-checking phase taking place.
Y5	= 1	Write-checking phase taking place.
Y6	= 0	Pattern in A register.
Y6	= 1	Zeros in A register.
Y7	= 0	Complement pattern being operated.
Y7	= 1	True pattern being operated.

Repeat Option

A repeat option is built into the loop, allowing one location to be cycled with the data pattern required. Set Y0 off and Y4 on, the H register to the address of the location under test, and the C register with the data required to be written and ROAR set up to 029. The machine will then run in a two-cycle read/write loop with data read out into the A register and written from the C register.

Local Storage Address Diagnostic

This test is another internal diagnostic selected by the diagnostic control switch. It checks that each location can be entered and retrieved without interference from any other addressable location. The address of each local storage word is written into its own location on the write phase and is read out and compared with the expected result on the read-checking phase. The test uses most of the microprogram that is used by the worst-case pattern test.

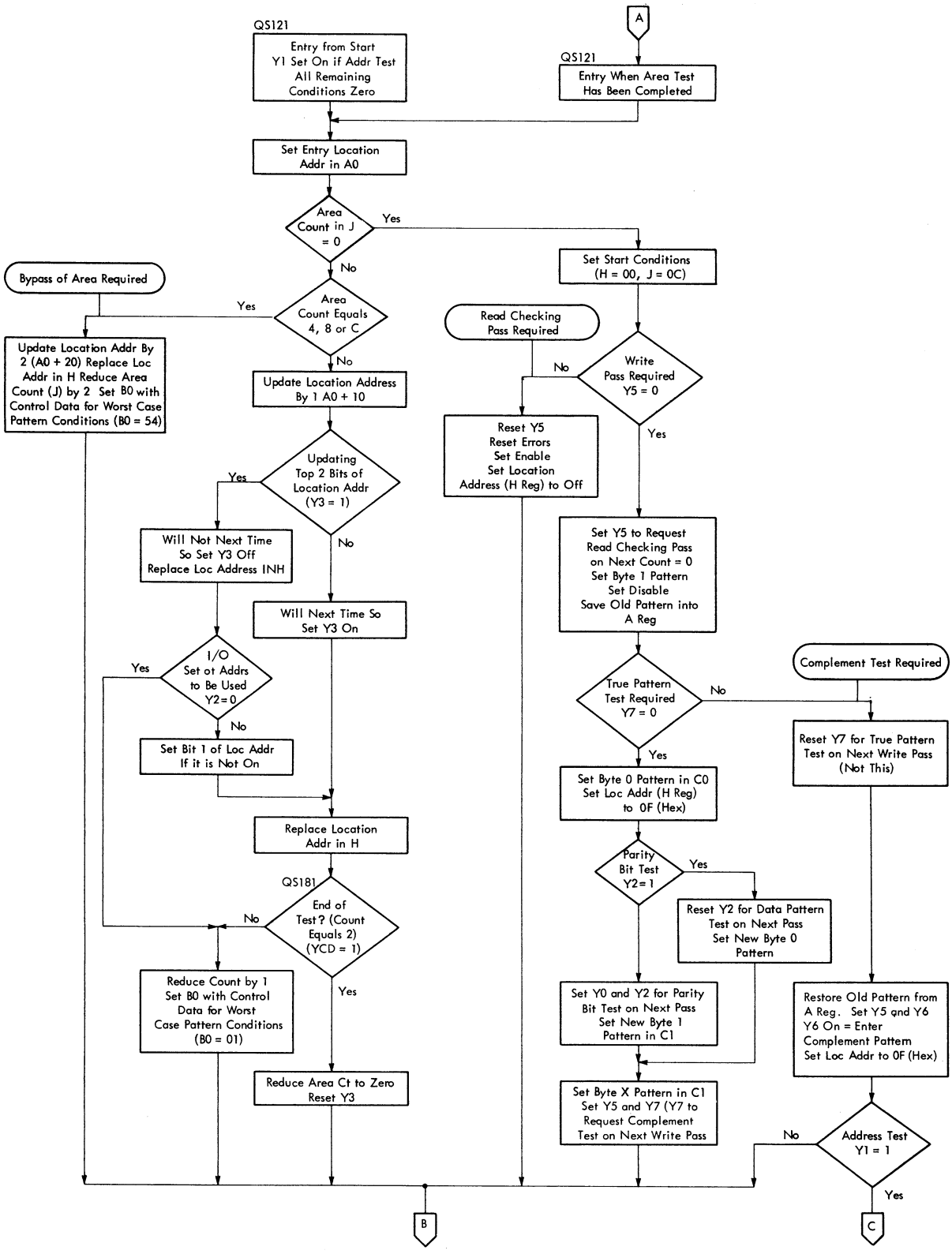


Figure 40. Local Store Diagnostic, Sheet 1 of 2

Entry Conditions: - Data to be Written in C
Pattern Control Data in B0
Address Set to High Order Location of the
Area to be Tested.

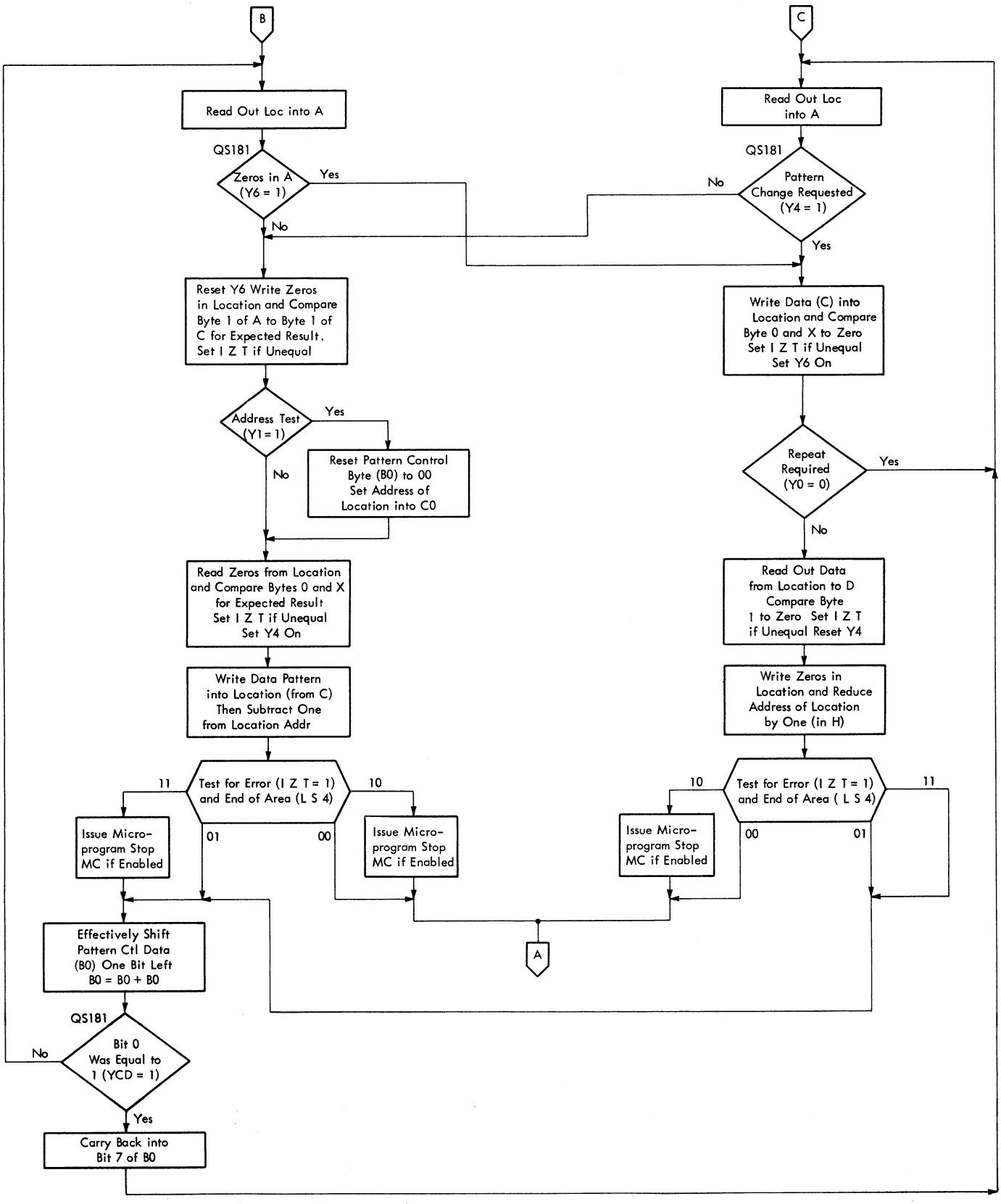


Figure 40. Local Store Diagnostic, Sheet 2 of 2

A flow chart of the diagnostic is shown in Figure 40. (See also Figure 912.) There are two routines. The first writes information in the 11 set of addresses. These are areas 0,2,3,4,6,7,C,E, and F (Figure 40). The second subroutine uses the 10 set of addresses which are areas 0,2,3,4,6,7,8,A, and B (Figure 39), i.e., the second test addresses the same area physically, but with theoretically alternate addresses. Each routine consists of a write phase followed by the read-checking phase, and is executed twice before the next routine is started. At the end of the second routine, the test restarts automatically at the first routine. There is no change of pattern required by this test so that only half the original loop is used, the B0 register being set to zero.

Method of Operation

The method of operation is as before, with the diagnostic control switch set on LS address position; depress the start switch with the machine in the manual halt state. The test then starts with the first routine and can be stopped only when an error is detected on the read-checking phase or when the system reset key is depressed.

Description

The address of each location is entered into byte 0 of its own location with byte 1 containing a constant for that area (J register). Even parity in any byte on the read-checking phase causes a hardstop condition to occur, and only the byte 0 is checked for the expected result (byte 1 is not being considered at all) which again results in a microprogram stop.

Because of changes set up by using Y1, the same uses are made of each register and staticizer as in the worst-case pattern test except that a more valid interpretation of Y2 is:

Y2 = 0 use the 10 set of addresses
Y2 = 1 use the 11 set of addresses

Main Storage Pattern Diagnostic

This diagnostic checks for sense and inhibit noise at full storage speeds.

Each location is checked in sequence as follows:

1. First loop
   - Read original pattern
   - Rewrite
   - Read second
   - Write complement pattern
2. Second loop
   - Read
   - Rewrite
   - Read
   - Read second
   - Write original pattern
3. Address + 2, got to next location.

There are four different phases cycling one after the other in this test:

1. Y7 not Y6, parity bits worst case complement pattern.
2. Y6 not Y7 data bits worst case pattern.
3. Y7 and Y6, data bits worst case complement pattern.
4. Not Y7 not Y6, parity bits worst case pattern.

Two complete runs through storage are completed for each phase:

First run with Y5 ON (no hardstop on error).
Second with Y5 OFF (hardstop on error – check pass).

Original patterns are used.

PHASE	BYTE 0	BYTE 1
Data bits worst case 1's pattern	1 11111111	1 11111111
Data bits worst case complement 0's pattern	1 00000000	1 00000000
Parity bits worst case 0's pattern	1 00000000	1 00000000
Parity bits worst case complement 1's pattern	0 00000001	0 00000001

For each phase the patterns are used as follows for a 16K area:

1. The original pattern is written into the first four bytes of storage.
2. The complement pattern is written into the four following bytes.
3. The original pattern is written into the four following bytes, and so on.

The second 16K area is written as the complement of the first, and the third in the same way as the first and so on until the end of the storage. End of storage is detected with SAT test, and the second run with Y5 ON (stop on error if any) is initiated.

How to Operate

To operate the test, the DSAB INTVL TIMER switch on panel C is down. The diagnostic control switch is turned to MS pattern and the system reset key is depressed to bring the machine into the manual halt state. The start key is depressed and ROAR forced to 009 to initiate the test.

NOTE: During the test avoid depressing the stop or interrupt keys. A PRI condition is checked during this test only to reset the MS address compare latch (scoping purposes).

Error Procedure

On a single error, a parity check occurs in both runs if the CPU check switch is not on disable. On double errors a microprogram stop occurs during the second run (Y5 off – check pass) if the CPU check switch is not on disable. In both cases the D register contains the data in error and the A register, the address in error. Stat Y3 determines the correct data. If stat Y3 is on, the correct data is in the form of a ONES pattern

contained in register B1. If stat Y3 is off, the correct data is in the form of a zero pattern.

Service Facilities

1. Loop on Any Phase – Any one of the four phases may be selected for looping by, performing a system reset, setting the J register to non-zero, and setting stats Y6 and Y7 according to the phase description above.

2. Loop on One Storage Location – To cycle any one storage location for scoping purposes, perform a system reset, set stop on ROS to stop at address 024, and start the pattern diagnostic. Set the H register to non-zero, the A register equal to the address to be cycled, the B0 register equal to LXXX XXXX, and B1 equal to the data to be written (B1 contents are written in both bytes in main storage).

3. The main storage pattern test can be used to check multiplex storage by turning on the Mpx storage toggle switch on console panel C, and using the same procedures as for main storage.

Use of Registers

A Register – address register.

B Register – B0 controls change of pattern every four bytes. It is loaded with 01011010 for worst-case phase or 10100101 for worst-case complement phase wrap-around shifted and analyzed for carry (QS151). B1 contains the ones pattern to be written; 0000 0001 for parity bits test and 1111 1111 for data bits test.

C Register – C0 is loaded with a fixed value (1100 0000), then OR'ed with A0 (top byte of address). If the result of the OR operation + 1 gives a value of zero, a 16K area has been completed.

C1 is used to update the main storage address.

D Register – data register.

H Register – H = 0 normal operation. H ≠ 0 loop on one storage location.

J Register – J = 0 normal operation. J ≠ 0 loop on one phase according to the setting of Y6 and Y7.

Stats Utilization

Y0 = 0 Normal operation.
Y0 = 1 Write, read, and check any pattern throughout storage (address test facility).
Y2 = 0 First loop.
Y2 = 1 Second loop.
Y3 = 0 Correct data zeros pattern.
Y3 = 1 Correct data ones pattern checking time.
Y4 = 0 Main storage pattern test.
Y4 = 1 Main storage address test.
Y5 = 0 Hardstop on error (check pass).
Y5 = 1 No hardstop on error (write pass).
Y6 = 0 Parity bits pattern.
Y6 = 1 Data bits pattern.
Y7 = 0 Worst case phase.
Y7 = 1 Worst case complement phase.

Address Test: Y6 and not Y7 byte 0 of address is written.
Y6 and Y7 byte 1 of address is written.
Y6 and Y7 byte X of address is written.

A flow chart of the diagnostic is shown in Figure 41. The microprogram is on CLD pages QS151 and QS191.

Main Storage Address Diagnostic

This diagnostic checks that each location can be entered and retrieved without interference from any other addressable location.

There are three different phases cycling one after the other in this test.

1. Y7 and not Y6 – both bytes of each storage location are written with byte 1 of its address.

2. Y6 and not Y7 – both bytes of each storage location are written with byte 0 of its address.

3. Y6 and Y7 – both bytes of each storage location are written with byte X of its address.

Each location in sequence is read, written, read again and rewritten.

Two complete runs through storage are completed for each phase:

First run with Y5 on (no hardstop on error).
Second run with Y5 off (hardstop on error).

An addressing error results in a microprogram error indication.

How to Operate

The DSAB INTVL TIMER switch on panel C is turned on (down position), the diagnostic control switch is turned to MS address and the system reset key is depressed to bring the machine into the manual halt state. The start key is depressed and ROAR forced to 00A to initiate the test.

NOTE: During the test avoid depressing the stop or interrupt keys.

Error Procedure, Register and Stats

See "Main Storage Pattern Test."

Service Facilities

1. Clear Storage – To clear all of main storage to zero, set stat Y3 on before starting the address diagnostic. The machine stops with a microprogram stop and the end of the diagnostic.

2. Write, Read, and Check and Pattern Throughout Main Storage – To perform this test, set stop on ROS to stop on address 026 and start the address diagnostic. When the machine stops at ROS address 026, set the address compare switch to process, set Y0, Y4, and Y5 on, set the desired pattern in the B register and Start.

A flow chart of the diagnostic is shown in Figure 41. The microprogram is shared with pattern test and is on CLD pages QS151 and QS191.

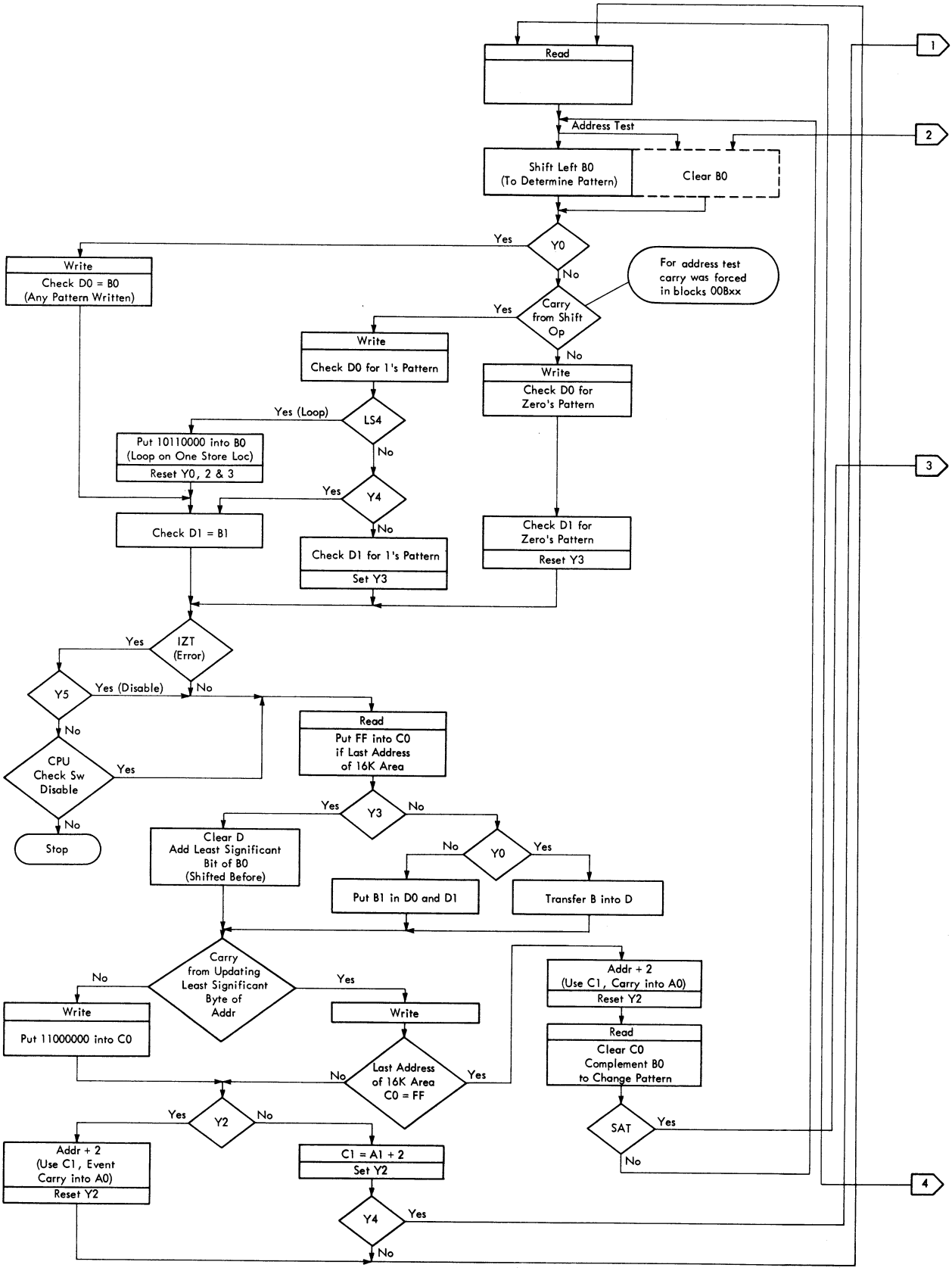


Figure 41. Main Storage Pattern and Address Test, Sheet 1 of 2

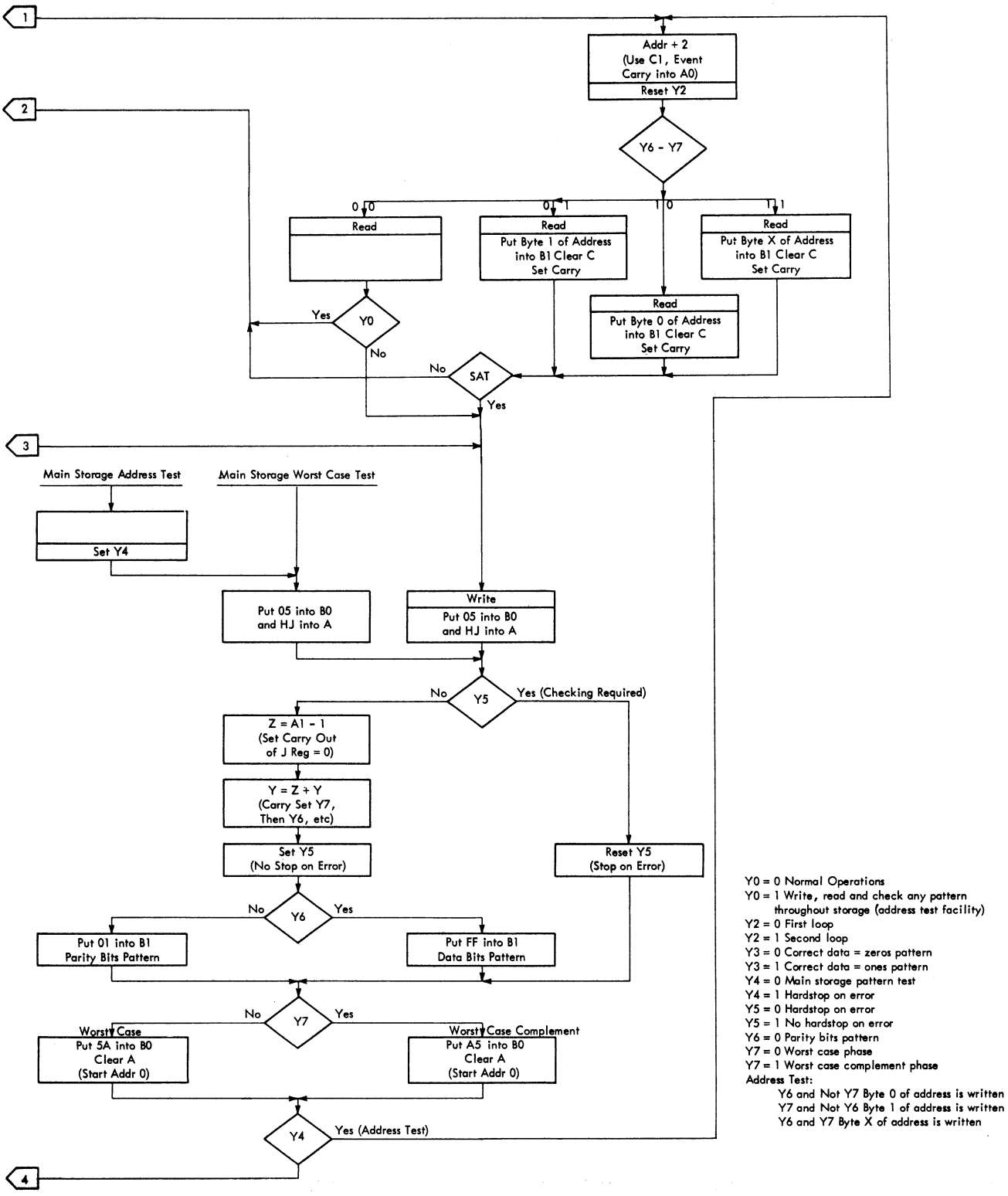


Figure 41. Main Storage Pattern and Address Test, Sheet 2 of 2

MS Validate

This diagnostic (CLD QS191) reads and writes sequentially through main storage. Correct parity is generated and automatically written into main storage. If the routine is run "enabled," parity errors cause a stop.

To run diagnostic:

1. Set diagnostic switch to MS Validate.
2. Press system reset.
3. Press start.

To stop diagnostic:
Press System Reset.

The operation is as follows: ROA1. is forced to 002 and Y2 is set by hardware when start is pressed with the diagnostic switch set to MS validate. 002 contains an instruction to read from MS and to add 2 to C1. Block 035 checks that C1 is not zero. Good parity is written back to MS by 135 (as it is not possible to write bad parity into MS); 135 adds 2 to A1 and puts the result into C1 and checks for valid storage address.

A branch now occurs on the storage address test.

If an invalid storage address is not present, 036 is entered. In 036, the contents of the C register are put into the A register and a carry is propagated into A0 if it was set in the previous block.

If an invalid storage address (which indicates the end of the storage) is present, 037 is entered. In 037 the A register is reset, ready to cycle main storage again. From both 037 and 036 the microprogram branches back to 002.

DUMP/UNDUMP

- **Provides a means of looping the dump and undump facilities.**

With the machine in the stop state and the Diagnostic Select switch set to Dump, logic circuits force ROS address 006 when the start key is depressed (QS051). The program forces a dump under microprogram control by use of the micro-order DUMP. The machine then performs one hardware cycle and six microprogram cycles to dump the CPU into local storage. At this point the machine tests ADR-I to determine the cause for the dump routine execution. Since the dump was not initiated by Mpx channel, ADR-I is not present; control is therefore transferred to the undump routine. This performs further six microprogram cycles and one hardware cycle to restore the machine to its original status. After a branch on Y7 condition, which is off in this case, the microprogram goes back to ROS address 006 and loops on this dump/undump routine.

NOTE: The Y7 stat test made in microinstruction is used when this test is entered by diagnose instruction. (Refer to "Diagnose Instruction – Start at any ROS Address"). The dump and undump routines as well as the detailed dump area in local storage are shown on CLD QA001.

Log Out

- **Log out is the technique of recording in main storage the status of the CPU and channels at the end of a microinstruction.**
- **Log out furnishes a record of the machine status at the time of an error.**
- **The main use of a log out is in troubleshooting intermittent failures.**

Cause of Log Out

1. A machine error is detected by hardware (i.e., a control, early or late check) and Y12 and Y15 are off and the machine is enabled (i.e., PSW bit 13 is a "1").
2. The log out pushbutton is depressed.
3. Either of the control signals LOG or ICC is given (i.e., when an error is detected by microprogram).
4. The diagnose instruction is used to force an error.

All specific checks are OR'ed in groups to set one of the three main check latches: control check, early check, or late check. The main check sets the master check latch. If Y12 and Y15 are both off and the machine is enabled, a log out occurs. A log out cannot occur during internal diagnostics, IPL, error hardstop, or during manual log out since Y12 or Y15 is on. Also no log out can occur during a run in disable mode. However, the main check stays on and if any interrupt introduces a PSW having bit 13 = 1, a log out is started. This occurs during the fetch PSW microprogram. Unmasking PSW bit 13 can allow a log out with only one main check as error indication.

The log button is effective in all modes if Y12 is off. Pressing the log button forces the Stop Clock Latch and Start Log Latch On. It simulates machine error handling by forcing a machine check interrupt and can be used to exit from a microprogram loop by a machine malfunction.

The signal is used in spare locations of TROS and in some invalid branches of the microprogram. It sets a control check. The ICC signal sets the ICC latch (channel check) and the late check. It is used in the channel microprogram.

In testing the check circuits, program errors are introduced in the data flow by the diagnose instruction. A log out is started and compared with a previous log out of normal conditions.

SEQUENCE OF LOG OUT

(See Figure 42)

1. Detection of the error or log button depressed.
2. Twelve logic cycles in which certain check latches and registers are temporarily stored in local storage.
3. Microprogram log out in which CPU and channel status are stored in main storage starting at location 80 hex. If a channel error caused the log out, only that channel is reset.
4. Reset errors and registers A and D.
5. CPU and channel check out program. If a channel error caused the log out, only that channel is checked.
6. Microprogram system reset. If a channel was reset during the log out, that UCW is reset during the microprogram system reset.
7. Machine check interrupt program.
8. Using the new machine check PSW a machine language routine is started.

When a check occurs, one of the main check latches is set (i.e., control, early, or late). The main check sets the master check latch. Stop half clock 1 prevents T1 and T2; the stop clock latch comes on, stop half clock 2 prevents T3 and T4. The next cycle will be the first of 12 logic cycles.

It should be noted that logic circuitry has been built into the machine especially for log out (Figure 43) Failure of this circuitry could give an invalid log out.

The start log latch is set at P2 of the first logic cycle (Figure 44). The next ten cycles are alternate read and write cycles to store five groups of checks and registers into local storage. Figure 45 details these groups. These checks and registers are generally those which are not accessible to the microprogram. Since the hardware log out uses parity bit positions as data bits, the parity in the R register and local storage can be bad. Therefore, all checking is disabled during the twelve hardware log out cycles. Note that the R register and LSAR parity bits only are logged out, not the contents. Y12 is set at P3 of cycle 3. This stays on, preventing channel dumps, until the new machine check PSW is loaded into the data flow. The T clock is started at the end of the 12th logic cycle. Address 00F is forced into ROAR and the microprogram log out proceeds from this point.

Figure 46 outlines the general sequence of the microprogram log out while Figure 47 details the data which is stored in main storage. The first few microinstructions store the D register and the A register into local store 0A and 09 respectively, since the D and A registers are used to log the data into main storage. The A register is set to 80 hex prior to entering the main loop in which information from register

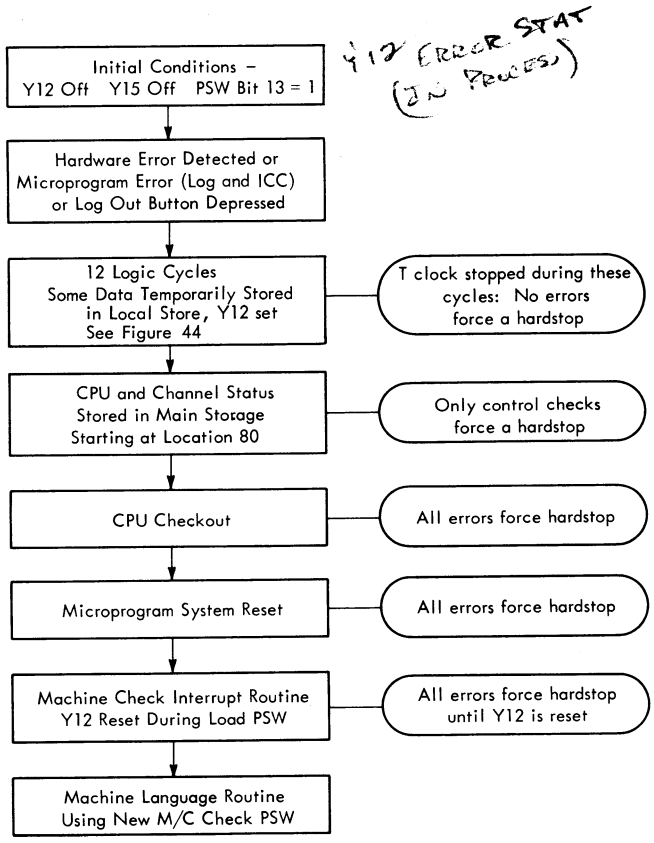


Figure 42. General Outline of Log Out

C is logged into main storage (Figure 48). Note that correct parity is generated before storing the data in main storage. Exit from the main loop is to one of 15 routines. In each routine, data to be logged is assembled in the C register. After each routine the main loop is entered again to transfer this data to main storage. Some routines are used only once while others may be used 12 times before moving on to the reset routine.

Only Control Checks force a hardstop during the microprogram log out. During the last pass of the microprogram log out, registers A and D are reset and all errors are reset.

Any error causes the machine to hardstop during CPU and channel check out, microprogram system reset, and machine check interrupt routine, up to the time Y12 is reset (i.e., when the new machine PSW is loaded into the data flow).

Log Out Validity

Normal Log Out is started by an error while the CPU is in the enable state, provided that the failure

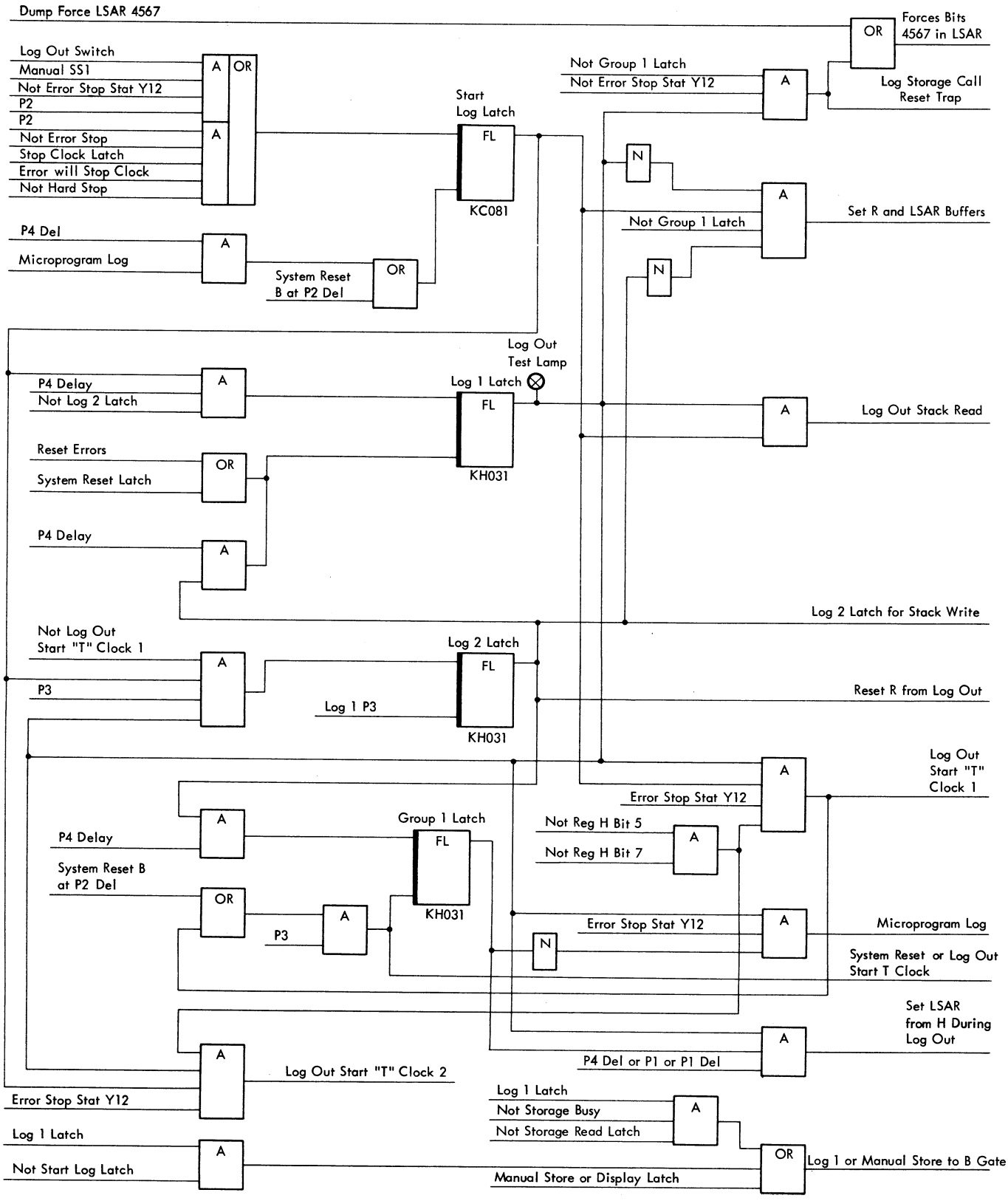


Figure 43. Log Out Latches and Controls

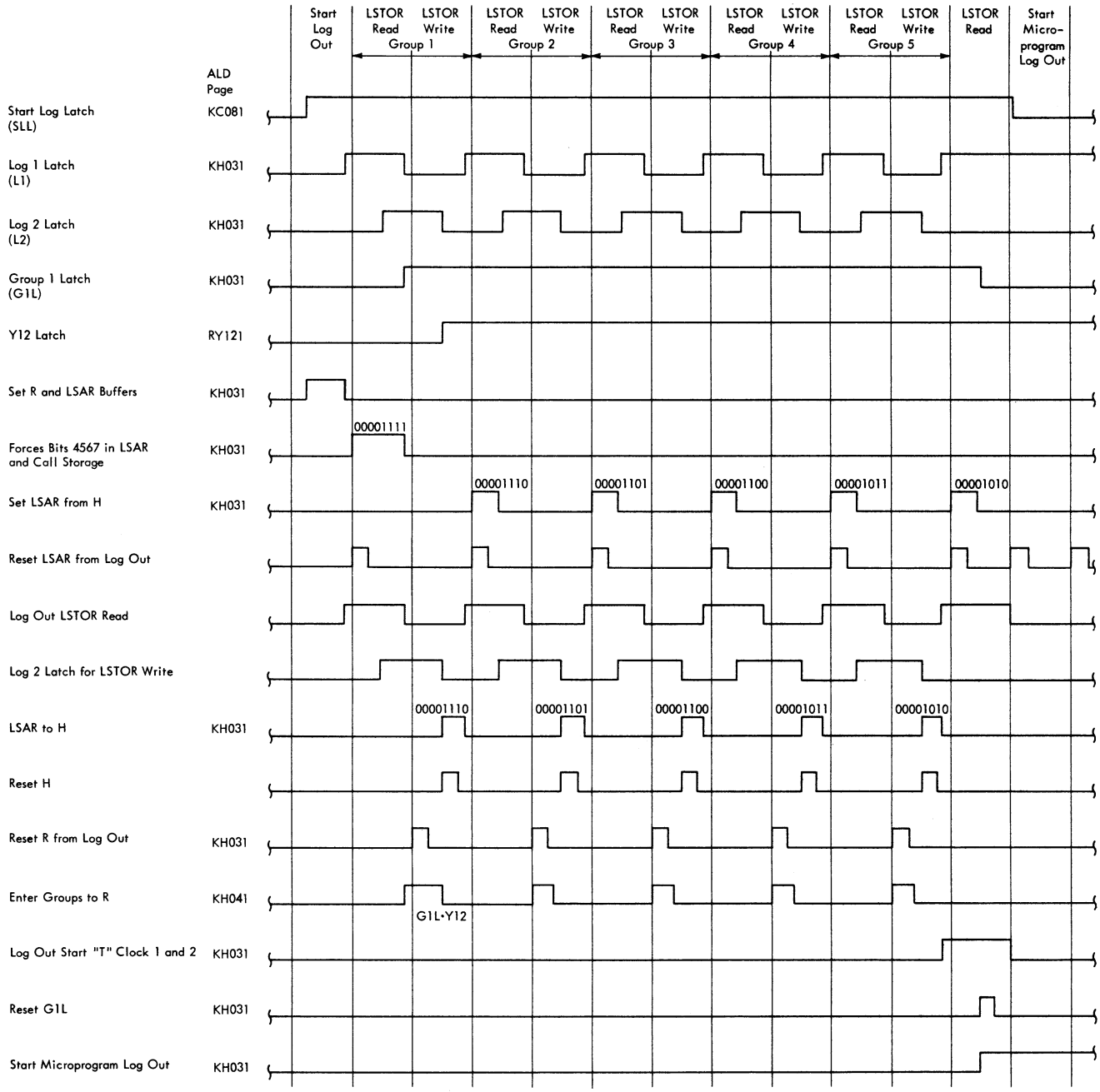


Figure 44. Hardware Log Out Timing Chart

did not affect the log out sequence and data. The source of the check is not always found in log out when:

1. The source is not logged out, e.g., the contents of LSAR. In this case, the error data may be found in the H or J register.

2. The course has been changed, e.g., a register which is a destination in the last T cycle. In this case the error data in the register could be replaced with valid data.

Main Check on Alone: The control, early, or late check can be on by itself for any one of these reasons:

1. An intermittent short affecting non-latched checks such as the 2W check.

2. Checking circuit failures.

3. Main check directly initiated (as by LOG).

	Bit	Group 1 Stored in LS 0F	Group 2 Stored in LS 0E	Group 3 Stored in LS 0D	Group 4 Stored in LS 0C	Group 5 Stored in LS 0B
Byte X	P	Not Used	Not Used	Not Used	LSAR Parity Check	EX Reg Bit P
	6	Not Used	Not Used	ROS Data Check	F Reg Bit P	EX Reg Bit 6
	7	Not Used	MSAB Parity Check	ROS Address Check	F Reg Bit 0	EX Reg Bit 7
Byte 0	P	H Reg Bit P	D0 Reg Parity Ck	RX Reg Parity Ck	F Reg Bit 1	P Reg Bit P
	0	H Reg Bit 0	D1 Reg Parity Ck	R0 Reg Parity Ck	F Reg Bit 2	P Reg Bit 0
	1	H Reg Bit 1	P Reg Parity Ck	PSA	F Reg Bit 3	P Reg Bit 1
	2	H Reg Bit 2	Q Reg Parity Ck	ISA	F Reg Bit 4	P Reg Bit 2
	3	H Reg Bit 3	J Decoder Check	I/O State	X ROS Bit B	P Reg Bit 3
	4	H Reg Bit 4	Stat Parity Ck	R1 Reg Parity Ck	ROBAR Bit 11	P Reg Bit 4
	5	H Reg Bit 5	LS Read Parity Ck	YCD	ROBAR Bit 10	P Reg Bit 5
	6	H Reg Bit 6	P Decoder Check	Y8	ROBAR Bit 9	P Reg Bit 6
	7	H Reg Bit 7	Q Decoder Check	Early Check	ROBAR Bit 8	P Reg Bit 7
Byte 1	P	R Decoder Check	SPLS Key Check	D/Y8 Check	ROBAR Bit P	Q Reg Bit P
	0	B Decoder Check	ALU Function Ck	2 Wire Check Bit 0	ROBAR Bit 7	Q Reg Bit 0
	1	C Decoder Check	2 Wire 1 - P Carry Ck	2 Wire Check Bit 1	ROBAR Bit 6	Q Reg Bit 1
	2	D Decoder Check	SPLS Data Check	2 Wire Check Bit 2	ROBAR Bit 5	Q Reg Bit 2
	3	H Increment Dec Ck	Skew Select Check	2 Wire Check Bit 3	ROBAR Bit 4	Q Reg Bit 3
	4	H Destination Dec Ck	2 Wire 0 - P Carry Ck	2 Wire Check Bit 4	ROBAR Bit 3	Q Reg Bit 4
	5	N Decoder Check	EX Reg Parity Ck	2 Wire Check Bit 5	ROBAR Bit 2	Q Reg Bit 5
	6	H Load Decoder Ck	ROAR Check	2 Wire Check Bit 6	ROBAR Bit 1	Q Reg Bit 6
	7	Control Check	Late Check	2 Wire Check Bit 7	ROBAR Bit 0	Q Reg Bit 7

Figure 45. Format of Hardware Log Out in Local Storage

4. Error while in disable mode, the log out starting when the PSW bit 13 is made a "1."

No Check On occurs when log out is started by the pushbutton.

Log Out Affected by the Failure: A failure which lasts for more than one cycle (as long as its check circuit is disabled) can affect the validity of the logged out data. For example, if a failure which lasts for a few cycles occurs in the main storage address circuits, the log out data could be stored outside the log out area, leaving some log out positions with old data.

Formatting and Editing

DEFINITIONS

Log out Hard Copy	Printed or punched copy of the log out.
Row Data	Log out as it is in main storage.
Dumped Log Out	Log out moved from main storage to another unit or hard copy, neither formated nor edited.
Formatted Log Out	Hard copy where data is assembled in meaningful groups. An example is shown in Figure 51.
Edited Log Out	Hard copy where the row data is decoded and printed in the most useful form. Titles and names of checks and registers are also printed. An example is shown in Figure 52.
Log Out Handler Program	Any program dealing with log out (dump formating and dump, editing and dump).
System Residence	Direct access storage device that has been assigned by the customer to the operating system as the file in which programs are stored.

Interpretation of the Log Out

The edited log out can be read directly since all registers and checks are labelled.

The formatted log out requires some preliminary work before the log out has any meaning. Figures 47 and 51 illustrate the use of the formatted log out.

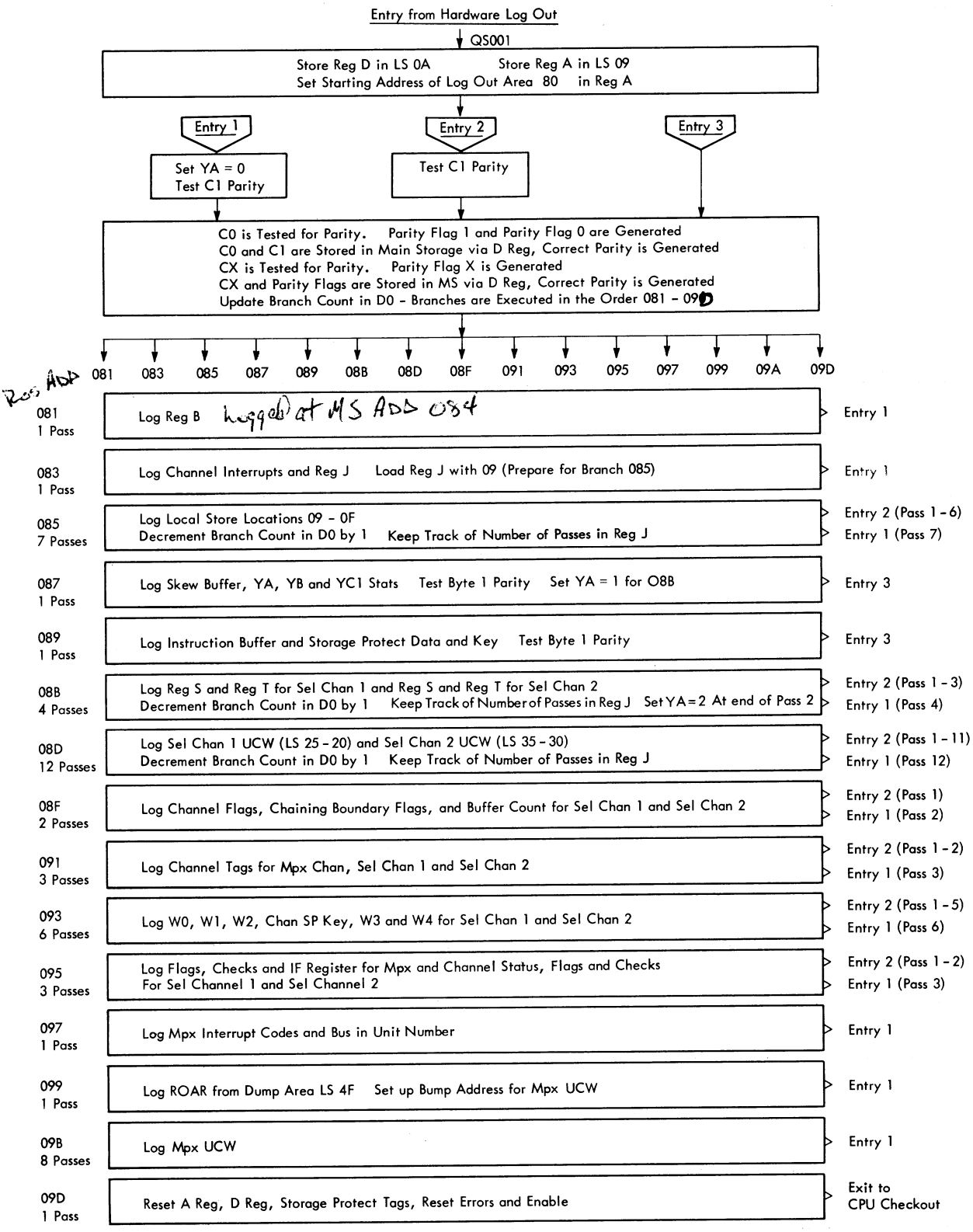


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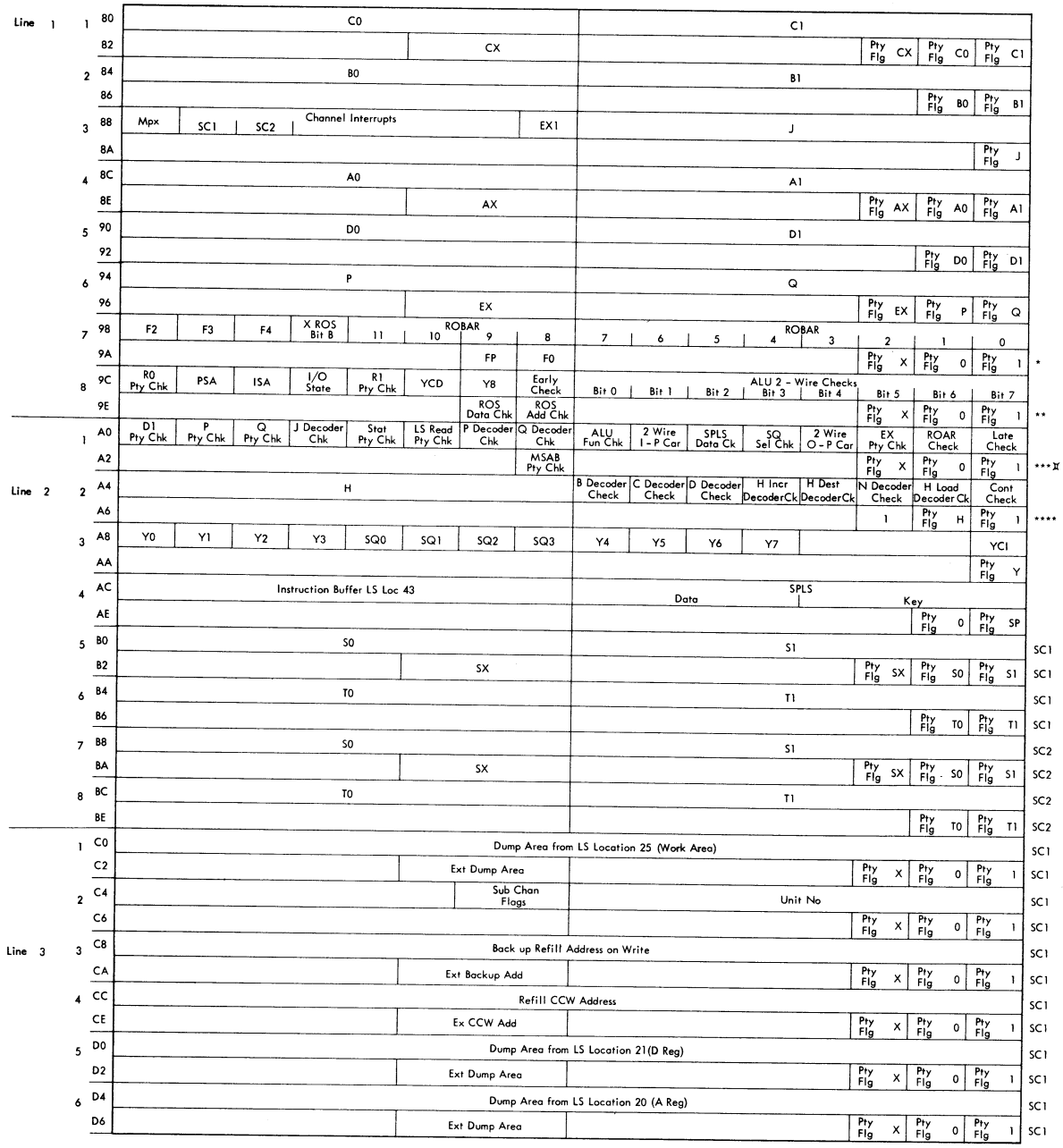
Figure 46. Chart of Microprogram Log Out



Parity flags indicate parity status of associated byte. If the flag is set then the byte had incorrect parity.

The formatted log out block is made up of four bytes (01 02 03 04).

The parity flags for these positions were derived by exclusive ORing the parity bits of bytes 03, 02, 01 **respectively with:**

*	LSAR Pty Chk	F1	ROBAR Pty
**	Ex 2-W Chk	Rx Pty Chk	D/Y8 Chk
***	0	D0 Chk	SPLS Key Chk
****	Not Used	Not Used	R Dec Chk

The results are byte 04. As an example: ¤

Parity of Bytes	03	02	01
Exclusive ORed with	0	D0 Chk	SPLS Key Chk
Results in the flags in byte 04 =	1	0	0

Figure 47. Main Storage Allocation for Log Out, Sheet 1 of 2

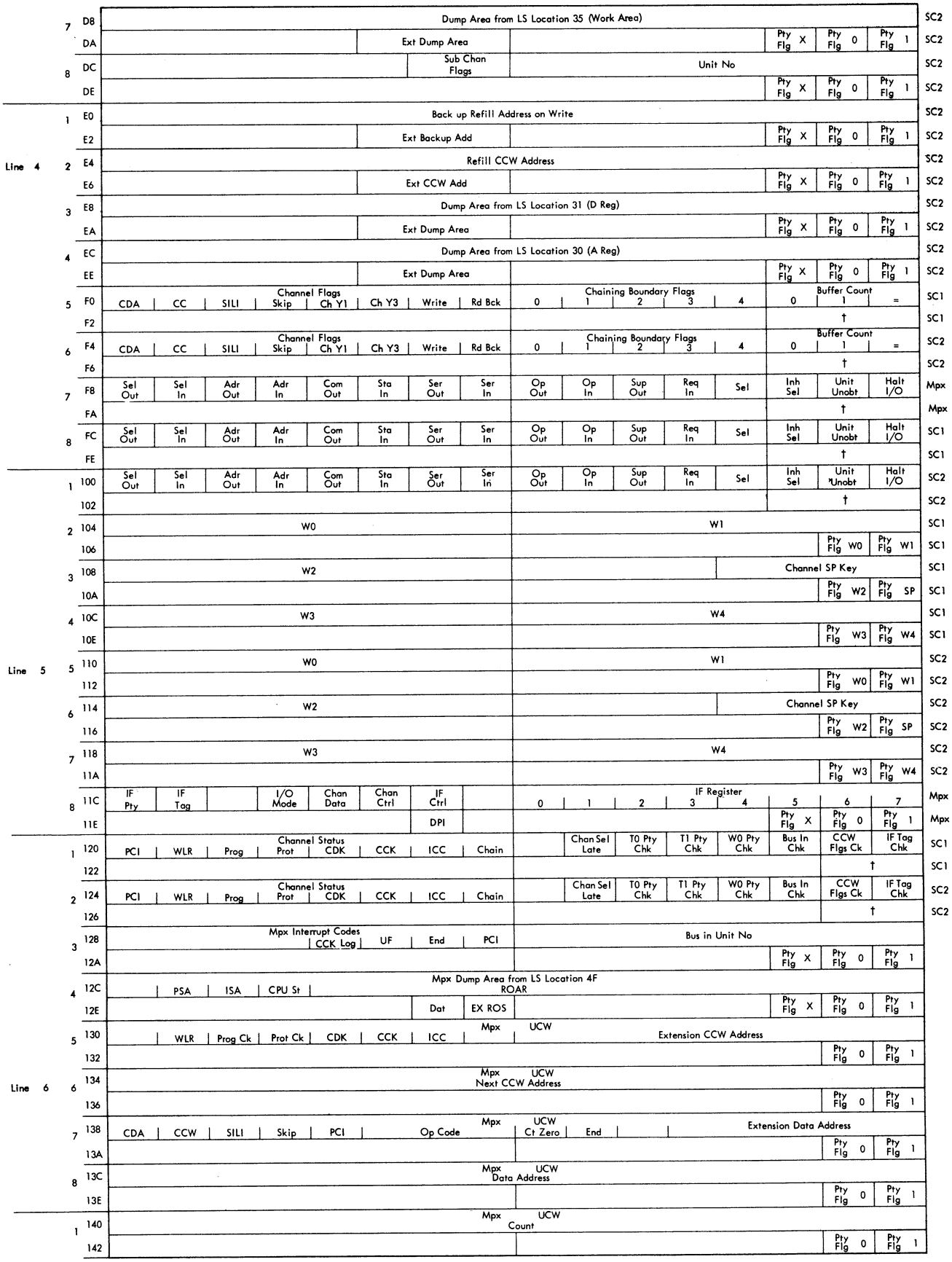
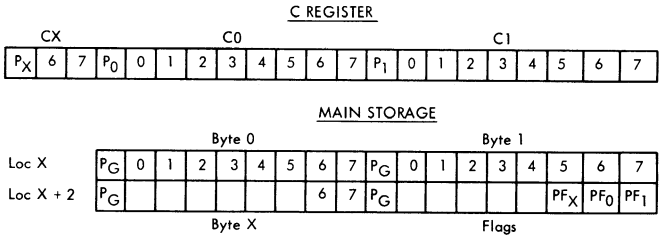


Figure 47. Main Storage Allocation for Log Out, Sheet 2 of 2



C0 bits 0 - 7 are stored in MS loc "X"; a parity bit is generated for these bits.
C1 bits 0 - 7 are stored in MS loc "X + 1"; a parity bit is generated for these bits.
CX bits 6, 7 are stored in MS loc "X + 2"; a parity bit is generated for these bits.
PF_X is a parity flag for byte CX. CX is checked for parity; if parity is good PF_X is 0; if parity is bad PF_X is 1; similarly PF_0 and PF_1 are parity flags for byte C0 and C1 PF_X, PF_0 and PF_1 are stored in MS loc "X + 3"; a parity bit is generated for these bits.

Figure 48. C Register to Main Storage

Figure 51 is divided into blocks of eight 4-bit characters. The blocks are numbered left to right, top to bottom, starting with "1." Each pair of characters in a block represents a byte of data held in main storage (e.g., block 1 represents the data in main storage hex locations 80, 81, 82, and 83, block 2 represents the data in main storage hex locations 84, 85, 86, 87, etc.)

The contents of the J register are located as follows: The J register is in block 3 (Figures 47 and 51). Block 3 is 00 37 00 00. The J register contains the value 37. Also the parity of the J register is correct, since the last character in the block is 0. Had this character been 1, the parity of the J register at the time the log out was started would have been incorrect and this could have been the cause of the log out (see Figure 49).

The contents of ROBAR are determined as follows: ROBAR is in block 7 of Figure 51 with the ALU function register, skew indicator, and LSAR parity check. The contents of block 7 of Figure 51 are 06, 53, 02, 06. Procedural steps to determine the contents of ROBAR (Figure 50) are:

1. Write down the printout of block 7, 06, 53, 02, 06. This represents the contents in main storage of byte 0, byte 1, byte X, and the flags respectively. (See Figure 47.)

2. Rearrange the data in the sequence byte X, byte 0, byte 1, ignoring flags 02, 06, 53.

3. Write down the binary bits as they would appear in main storage showing the parity that was generated for each byte:

BYTE X	BYTE 0	BYTE 1
P01234567	P01234567	P01234567
000000010	100000110	101010011

Note that byte X bits 0-5 are always zero. These zeros are padding and can now be ignored.

4. Write down the binary bits shown in step 3 above, ignoring bits 0-5 of byte X.

BYTE X	BYTE 0	BYTE 1
P07	P01234567	P01234567
010	100000110	101010011

5. Decode the flags. In this example 6 = 110. Write the flags underneath the parity bits.

6. Exclusive OR the flags with the parity bits in step 4.

7. Write down the actual contents stored in LS by combining the parity bits formed by step 6 and the data bits from step 4.

BYTE X	BYTE 0	BYTE 1
P67	P01234567	P01234567
110	000000110	101010011

8. ROBAR is byte 0 bits 4-7, and byte 1 bits P, 0-7 (See Figure 50). Since the parity bit of byte 1 is also the parity bit of ROBAR, the value of ROBAR is 0110 0101 0011 (i.e., 653), and ROBAR is in correct parity.

Note also that the function register is 00000 (i.e., OR); the parity given by byte X bit 6 is correct. Further, the LSAR check latch was on – byte X bit P.

Systems Environment Recording, Editing, and Printing (SEREP)

The SEREP program is intended to be loaded manually, via IPL, on the occurrence of a machine check interrupt or solid I/O error. The program does not require any other programs to be present in storage. Basic machine requirements are a minimum storage size, an output device, and a program loading device. The program requires the use of a control card to obtain required systems information listed below:

1. Output device address
2. Pseudo IPL device address (if desired)
3. Channel type

One control option is provided for a pseudo IPL to be executed at the completion of the program to allow the operation program IC to be re-initialized automatically at the completion of an edited output. The channel type allows the program to associate a particular channel assignment with a type of channel.

The wait loop can be entered with any of five conditions:

1. IC equal to 00000 if a pseudo IPL is not to be performed at the completion of the SEREP program.
2. IC equal to 00001 if the specified output device is not operational or a unit check occurred when the device was addressed.
3. IC equal to 00003 if an unexpected program interrupt occurred.
4. IC equal to 00007 if the specified input (pseudo IPL) device is not operational or a unit check occurred when addressed.

Block 3 is 0_1 0_2 3 7 0_5 0_6 0_7 0_8

Main Storage Locations and Data

88	P	0_1				0_2				P	3				7				89
		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	
8A	P	0_5				0_6				P	0_7				0_8				8B
		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	

Notes: The "P" bits are not indicated in the block. These bits should be correct parity bits since they were generated during the log out.
Log 8B bit 7 is 0. Therefore parity of J Reg was correct at time of log out

Figure 49. Determining the Contents of the J Register

1.

Byte 0	Byte 1	Byte X	Flags
0 6	5 3	0 2	0 6

2.

Byte X	Byte 0	Byte 1
0 2	0 6	5 3

3.

P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	1	0	1	0	0	1	1

4.

P	6	7	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7
0	1	0	1	0	0	0	0	0	1	1	0	1	0	1	0	1	0	0	1	1

5.

1		1		0	

6.

1		0		1	

7.

P	6	7	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7
1	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	0	1	1
P	P	0	1	2	3	4	12	11	10	9	8	P	7	6	5	4	3	2	1	0
LS AR	Function RG						X ROS	ROBAR												

ROBAR is 0110, 0101, 0011, ie 6, 5,3
X ROS bit 5 is 0
Function reg is 00000, ie OR no skew
LSAR parity check is 1.

Figure 50. Determining the Value of ROBAR from Formated Log Out

```
00000200 FFFF0000 00370000 00000000 00290000 00000000 06530206 10000005
00010006 36000005 00000000 4A300000 00000000 00000000 00000007 00000003
00000007 00000000 00000000 00000000 00000007 00000007 00000007 00000000
00000000 00000000 00000007 00000007 00050003 00000003 04C00001 00A00003
00000003 00000003 00000002 00000003 00000007 00000007 00000007 16000200
00000001 00000003 02090000 B4690000 00000000 00000000 00000000 00000000
0000000
```

Figure 51. Formatted Log Out

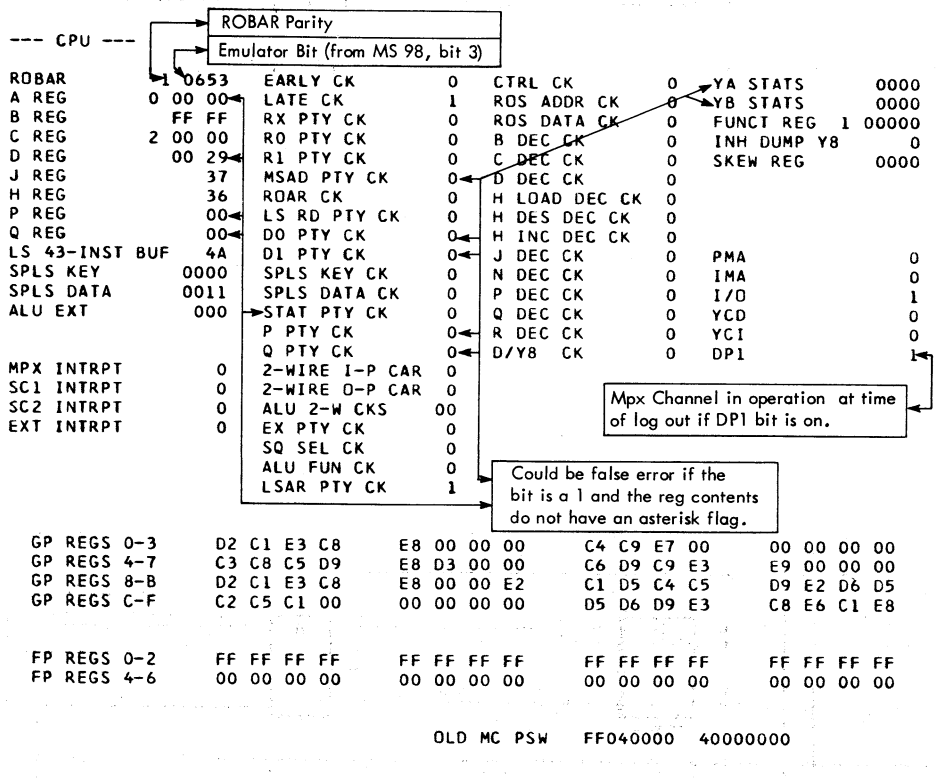


Figure 52. SEREP Log Out, Sheet 1 of 2

5. IC equal to 0000F if there is no control card following the SEREP program deck.

There are five types of print out. The SEREP program uses the new machine check PSW byte 73 hex to determine the type of failure encountered by the operating program as follows:

BYTE 73 HEX CONTENTS	TYPE OF ERROR	TYPE OF SEREP PRINT-OUT
Not 0F, 1F, 2F or 3F	CPU	Edited Machine Check Log
0F	I/O Channel	I/O Inboard Data
1F	I/O Device Unit Check	I/O Outboard Data
2F	I/O Test Channel	I/O Test Channel Data
3F	I/O Device Not Operational	I/O Device Not Operational Data

NOTE: Byte 72 hex indicates that the system was operating in emulation mode when the failure occurred.

Initial Program Load

The loading of a program from any I/O device attached to any channel is described as follows:

The I/O device address is set up in the load unit switches on panel H. The left switch selects the channel. The center and right switches select the unit on the channel.

The load button is active only in the stop loop. When the load button is depressed, this sequence of operations occurs:

1. Hardware system reset is forced.
2. CPU and channels checkout program is executed, followed by a microprogram system reset.
3. Main storage is validated.
4. The load stat (Y15) is set by hardware to control the load operation, and force a hardstop on errors.
5. A CCW is assembled by the microprogram, starting at main storage location zero, with the format 0200

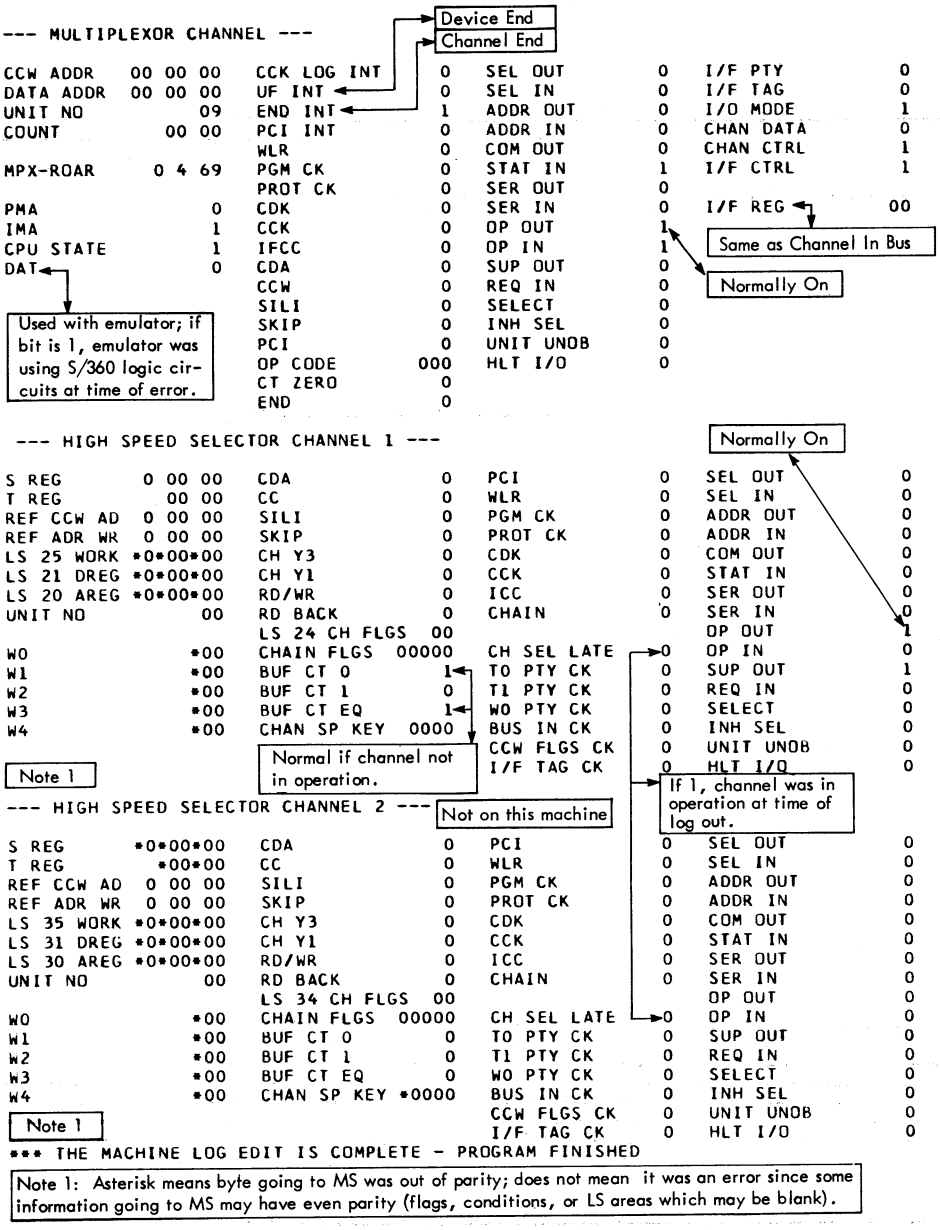


Figure 52. SEREP Log Out, Sheet 2 of 2

0000 6000 0018 (read, address zero, cc and SILI flags on and a count of 24 bytes).

6. A UCW is formed from this CCW (0200 0000 6000 0018) and the I/O device selected. The assembled CCW causes the initial program loading PSW to be read into location zero (over-writing this CCW), the initial program loading CCW1 into location 8 and the initial program loading CCW2 into location 16.

7. Command chaining from the assembled CCW to the initial program loading CCW1 (read into main storage location 8), occurs automatically after the PSW and the two CCW's are read in. From this second CCW onwards, further activities are completely up to the program, chaining could be programmed to the next CCW, and so on.

8. Between fetching CCW's, the microprogram loops in the IPL wait loop. Data service is obtained by microprogram interrupts (dumps) for the multiplex channel or buffer service break in for the selector channels.

9. CCW's and program instructions continue to be read in as long as the CCW being used has the CC flag on.

10. When a CCW no longer specifies chaining, the microprogram routine continues. If no errors are present, the initial program load PSW is loaded from

main storage position zero into the data flow (current PSW), the load stat (Y15) is reset, and the execution of the program starts under control of this PSW.

Possible Causes of Microprogram Hang-up for Errors Occurring During IPL

LOOP ON HEX ADDRESS	CAUSE
50D	Invalid channel number (greater than 2)
4CB-4F8	Two different causes:
	1. Unit status byte does not have the channel end bit on.
	2. Unit status byte indicates some errors (attention, control unit end, busy, unit check or unit exception).
4FB	Error byte indicates some errors (WLR, program check, protection check or interface control check).

A machine status chart followed by a flow chart show the IPL operation for multiplex channel and is given in the following pages.

IPL Machine Status Chart for Multiplex Channel

CAS PAGE	ROBAR	IF TAGS (s = set r = reset)	CHANGE OF STATS	LSAR	REG H	REG J	COMMENTS (ALL LOC IN HEX)
QC121	444		ERROR, LOAD (entry conditions)				Enter from system reset into Load routine.
	467		rERROR	08		07	Emit 8 into A, to form IPL forced CCW.
	44D		sMAN	07		06	Clear LS 07, decr A by 2 (A = 0006).
	44E			06		05	Clear MS 0006, clear LS 06, create CCW count in B1 (18).
	45E			0A	0A	05	Create CC and SILI flags in C0 (60).
	45F		sMAN	05		06	Write 0018 into MS 0006 (count).
	44D		rMAN	06		05	Clear LS 06, decr A by 2 (A = 0004).
	44E			05		04	Clear MS 0004.
	45E			0A	0A	04	
	45F		sMAN	04		05	Write 6010 into MS 0004 (flags).
	44D		rMAN	05		04	Clear LS 05, decr A by 2 (A = 0002).
	44E			04		03	Clear MS 0002, clear LS 04.
	45C			41		41	Reset D reg, set 02 into C reg.
	45F		sMAN	41		42	Set 02 into B0 from C, write 0000 in MS 0002 (data address).
	44D		rMAN	42		41	Decr A reg by 2 (A = 0000).
	44E			41		40	Clear MS 0000.
	45E			0A	0A	40	Set B into D = 0200 (IPL read command).
	45F		sMAN	40		41	Write 0200 into MS 0000 (read command).
Up to here a CCW has been loaded into MS 0000. This CCW contains an IPL read command, data address 0, count = 24 bytes, command and SILI flag.							
	44C		rMAN	2A	2A	41	From load address sw set unit addr into B1 and chan addr into B0 bits 5, 6, and 7.
	44F		sID	2A	2A	41	Clear LS 2A (interrupt buffer), mask chan number and put it into B0.
QB101	50D			00	2A	41	IPL failure loop if chan number too big.
QC121	50C			05	2A	06	Store chan and unit number into LS 05.
	4CF			06		07	Store unit number into LS 06, Set Y2 Y3 = chan number.
	4D6			2A		07	Store unit number into interrupt buffer, test if single or multiple unit.
QC101	4FC				2A	07	(Single unit) skew unit number to generate UCW addr, reset interrupt request.
	4E0		rIZT-IDQ	42	42	07	Complete UCW addr, test Y4 = 0 for IPL.
QC121	560	SUP Out	rID	07	42	07	Set interrupt request, write UCW addr into LS07.
Up to here the load address switches have been read to give channel and unit number. Y2, Y3 have been set to 00 (Mpx channel). CPU working area has been loaded with: 07 = UCW address (generated from unit number). 06 = unit number. 05 = channel and unit number. The interrupt request latch has been set and the interrupt buffer loaded with the IPL unit number to prevent other devices generating interrupt.							
QC121	554		r4, 5, 7	07	42	06	Clear D and B1. Set select latch (SEL).
QB131	558			06	42	07	Clear A, branch on Y6 (off for Mpx).
QB501	575			07	42	08	Read command from MS 0000, Clear B.
QB131	564						Set CPU state, test invalid addr.
	578				42	08	Write back command to MS.
	54E			08	42	08	Incr A by 2 (A = 0002), clear LS 08, test end of loop? (no).
	568			08		09	Read data addr from MS 0002, put command into B0 and extn addr into B1.

CAS PAGE	ROBAR	IF TAGS (s = set r = reset)	CHANGE OF STATS	LSAR	REG H	REG J	COMMENTS (ALL LOC IN HEX)
	564						Data addr in D reg, test invalid addr.
	578						Write data addr back to MS, put data addr into C from D (extn addr into CX from B1).
	54E			09		09	Incr A by 2 (A = 0004), clear LS 09, end of loop (yes).
	56A			09		08	Put data addr into LS 09, test command for TIC.
Command and data address have been fetched from CCW at location 0. CPU working area has been loaded with: 09 = compressed data address. Command is in B0.							
	571			08		06	Read flags from MS 0004, put command (02) into C1, set skew reg to 4 (read op).
QB141	576		sID	06		04	Read unit number from LS to B1, clear C0, set I/O state, test Y6? (off).
	561		rID			04	Write back flags to MS, set flags into B0.
	553			04		05	Incr A + 2 (A = 0006), put command into D1, set CPU state, L2≠0? (no).
	559			05		06	Read count from MS, put command into C1, check bits 37–39 = 000.
	556						Add op code (from skew) and flags and put them into B0, write? (no).
	54C						Test for skip? (no).
	54D			06		07	Write back count to MS, write count into LS 06, test D1 for zero count.
	553			07		08	Incr A + 2 (A = 0008), set command into D1, set CPU state, L2≠0? (yes).
	55B		s4				Allow for A1 carry, set flags and op into C0, unit number to C1, test for CC? (Y6) and prog check? (Y5).
	5D8		r4	08		07	Write refill addr from A reg to LS 08; clear B0; set I/O state. Set select latch (SEL).
Flags and count have been fetched from CCW at location 0 and checked for validity. CPU working area has been loaded with: 06 = count. 08 = refill CCW address. Command has been recoded and put with flags into C0, unit number is in C1.							
QB121	5E4						Add 1 to B1 for IF time out, Test DU/IF, test Y4? (off).
	5D0						Allow for B1 carry, test carry from B0 = ICC.
	5E4						Add 1 to B1, test DU/IF, Test Y4 (off).
QB121	5D0						Allow for B1 carry, test carry from B0 = ICC.
	5E4						Add 1 to B1, test DU/IF, test Y4? (off).
	5D1						Clear B0, put unit addr on bus out.
	5E3	ADR-O	s4				Set ADR-O and Y4 to signify addr set.
	5E4	SEL. OUT					Test Y4? (on) and DU/IF, add 1 to B1.
	5D2	OP-I					Test ADR-I and STA-I? (off), set unit number to D0.
	5E0	ADR-I					Add 8 to B0 for initial sel time out, test YCD = ICC.
	5E4						Test Y4 and DU/IF (DU/IF = unit unobtainable).
	5D2						Test ADR-I and STA-I (ADR-I = on).
	5E2			48	48	07	Addr on bus in to B1, command to C1.
Interface was free, address out has been given, address in is now on bus in.							
	5FB		sID	48	48	07	Test address match (ALU≠0 = ICC), set command to bus out.
	5F4	CMD-O		48	48	07	Set Y2Y3 into B0, clear LS48 (I/O instr flag).
QB151	5C9			48	48	07	Set I/O instr flag (FF for Mpx) into D1, set CPU state, test Y0 = HIO, Y7 = TIO.
	5CC		rID	48	48	07	Write I/O instr flag to LS 48, test Y2 Y3 for chan number.
	5FE		s1	07		08	Set storage protect key into B0 (bits 0-3), load A with UCW addr set I/O state.
	57C			26			Clear LS 26, read count byte from UCW 0 (Mpx stor), set storage protect key into skew buffer from B0.
	54A			27			Clear LS 27, set storage protect key into SPLS data and key registers.
	54B			29			Clear LS 29, write back count, write key into SPLS.
	57E			27			Write UCW addr into LS 27, Incr A + 7 (A = UCW3).
	57D			08		09	Put flags and op code into B0, read refill CCW addr into C, clear UCW3.
QB181	57F				20		Set refill ext into AX, Set C into D.
	5BE			09		07	Set data address into C, write D (refill CCW addr) into UCW3.
	5BF			06		06	Incr −A + 1 (A = UCW4), set count into D.
	5B5			29			Store count into LS 29, test Y5 = prog check.

CAS PAGE	ROBAR	IF TAGS (s = set r = reset)	CHANGE OF STATS	LSAR	REG H	REG J	COMMENTS (ALL LOC IN HEX)
	5BC						Set refill ext into D1, clear D0.
	5B0			26	26		Write refill ext into UCW4, set flags and op code from B0 into C0, write data addr into LS 26.
	5B1			28		28	Clear LS28, clear B0.
QB181	5B2			28		29	Write unit number into LS28, set unit number into C1, test for STA-I? (off).
QB151	5F2						Test YCD = ICC.
	5FC						Add 8 to B, set I/O state, test Y4? (on) and STA-I? (off).
	5F2	STA-I					Test YCD = ICC.
	5FC						Add 8 to B, set I/O state, Test Y4? (on) and STA-I? (on).
	5F3						Put status into D1, number into C1, set CPU state. Test Y0 = HIO, Y7 = TIO.

Adress in checked, command out sent and status in now on bus in.

UCW contents

UCW 3 = refill CCW address

UCW 4 = status and extend refill CCW address

Data in CPU working area transferred to Mpx working area

26 = data address

27 = UCW address

28 = unit number

29 = count

	5F8		sID				Check status = 0. Test Y5 = program check.
QB161	5B8	SVC-O	rID				Set service out.
	589						Set I/O state, reset C1, test for SVC-O or CMD-L.
	58A						Add 4 to B0, keeps looping until SVC-O falls, YCD = ICC.
	588		sID				Set B0 to FF, set CPU state, test Y4? (off) and Y1? (on).
QB171	599		s5	29		29	Set UCW op code into YB stats, test previous setting of Y6 and Y5? (off), read count from LS 29 to B reg.
QB181	5B4			2A			Read interrupt buffer to D, set 40 into A1, set I/O state, test interrupt req? (on).
	6F7			2A			Write back interrupt buffer (2A LS), check for valid chan number (ALU≠0 = invalid).
	6DA		s4	26	26		Decr B1 by 1 (count), read data addr from LS 26 into A, test Y5? (on).
	6F5		r5	29		27	Write op code and flags into LS29, allow carry from B1.
QA191	6F0			26			Write data addr into LS26, clear C0, test SVC-I and OP-I? (off).
QA231	670		s0, 1	27		27	Read UCW addr from LS27 into A reg, incr B1 + 1 (count), test STA-I? (off).
	660		s6	27		28	Set CIB (chan errors) to C0, allow carry from B1, read count from UCW0.
	6A1			28		29	Test for chan errors in C0, put count from B into D.
	689		rID	29			Read flags op code into B, write back count into UCW0, test Y4? (on).
	6BE						Set A (UCW addr) to D, incr A1 + 4, test SVC-O or CMD-O.
	69D			26	26		Read UCW2, read data addr from LS26 to C, save end reached flag in B1, test Y5? (off).
	69A		r4				Set op code, flags and ext data address into D.
	691			26	26	29	Write D into UCW2, write data addr to LS 26, put A1-4 into C1.
	6BC						Put C1 + 2 into A1 (A = UCW1), test interrupt req.
	63E		sID	48		48	Read start I/O instr flag from LS48 to C, test B0 for PC1 flag, clear chan.
	624			26	26		Read data addr from LS26 to D, test C for start I/O instr flag? (yes).
QB171	636		rID	48		47	Clear start I/O instr flag (LS48), Put 01 into B1, Test load stat? (on).
QC121	4F6		r0, 1				Reset A reg, set CPU state, test ALU≠0.

This is the IPL wait loop. When I/O device calls for data service, the CPU dumps from this ROAR address. After data service CPU undumps back to this loop. When device calls for status in with command chaining, the start I/O routine is entered again, if device end was present. After a LDB test, the CPU undumps and returns to the wait loop.

When I/O device calls for final status service (no command chaining anymore), the CPU dumps, analyzes the status and, if no errors are present, the function register is set with add. The CPU then undumps, and, because the function register now says ADD, ALU≠0 is present. This allows exit from this block, the UCW is transferred from Mpx storage to local store, the status and error bytes are analyzed and the initial load PSW is loaded from main storage position zero into the data flow (current PSW).

The data, status and command chaining services use normal multiplex microprogram.

Check points are listed:

CLD PAGE	ADDRESS	DESCRIPTION
QA251	68F	Data service complete. Terminal status now on bus in.
QC121	4F7	IPL end reached. Indirect function has been changed to ADD.
QC111	420	CSW information taken from UCW.
QC111	4F8	Status assembled.
QC091	4D0	PSW loaded from location 0.

1401/1460 Compatibility Feature

Console Facilities

Address Keys: If the DAT latch is off and the thirteenth bit of ROAR is on, the 1401 address translator is on. The address keys can now address 1401 storage.

Data Keys: Bit 7 of byte EX, bits 4-7 of byte 0, and bits 0-7 of byte 1 of the storage data keys are used to set a 13-bit ROS address into ROAR. Bit 6 of byte EX is used to set/reset the DAT latch.

R-Bus Selection Switch: The contents of ROAR can be displayed in panel lights in the order mentioned under data keys.

Stop on ROS: The machine stops at the end of the cycle in which the contents of ROAR (13 bits) and the data keys (EX bit 7, byte 0 bits 4-7, byte 1 bits 0-7) were equivalent.

Stop on Main Storage: The machine stops during I-fetch. When the main storage address (either model 40 or the 1401 compatibility HDDD) and the address keys are equivalent.

1410/7010 Compatibility Feature

2040 Console Facilities

The 2040 console provides access to the 1410 compatibility feature functional units and the emulator program.

Storage Address Keys

The 1410 address translator is turned on by a 1 in ROAR bit 12 and the DAT latch off. With the address translator on, the storage address keys access 1410 emulated storage.

Storage Data Keys

Position 7 of byte EX, positions 4-7 of byte 0, and positions 0-7 of byte 1 of the storage data keys are used to set the 13 bit ROS address into ROAR. Bit 6 of the EX byte is used to set/reset the DAT latch.

R-Bus Selection Switch

ROAR is displayed in the console indicator in the same order as described under "Storage Data Keys".

Stop on ROS

The system stops at the end of the cycle in which the ROAR contents and the storage data keys are equal.

Diagnose instructions in the emulator program branch to ROS address 0740. Because 0740 is a forced address, it cannot be used in a "stop on ROS" operation. Use the next ROS address 14DA when analyzing control transfers between the emulator program and microprogram routines.

Stop on Main Storage

The system stops in I-fetch when the 1410 address (ODDDD) and the main storage data keys are equal.

The following schedule shows recommended preventive maintenance action.

PM ROUTINE 6

CODE U	CODE R	LOCATION OPERATION	FREQUENCY	ACTION
1		Blowers and Filters	As required	Inspect, repair, or replace
2		Power Supply	12	Check EPO
3		Use Meter	3	Run F38F Diagnostic

Notes:

1. See System/360 General Service Aid No. 4 for part numbers of data, listings, and write-up.
2. To check the EPO switch, power down the CPU, pull the EPO switch, and try to bring power up on the system.

Check Points for Voltage and Timing

Voltage levels and ripple should be checked with a digital or high-precision voltmeter (Branch office tool, P/N 461079) using meter jacks on the internal CE Panel; ripple should be scoped. The meter jacks on the CE panel should be used along with the select voltage switch as the input for scoping.

NOTE: When using scope or DVM on meter jacks, leads must be switched when selected voltage changes polarity, to avoid grounding the voltage.

	VOLTAGE	TOLERANCE
	−3	±0.12v
	+3	±0.12v
	+6	±0.10v
	+18	±0.72v
	+24	±0.96v
	+48	±1.46v
MS/Vxy, MS/Vz	Refer to Main Storage section for operating point.	
PS/Vxy	+1.80	±0.02v
PS/Vsl	+3.20	±0.03v
LS/Vxy	+3.80	±0.10v
LS/Vm	−6.95	±0.07v
LS/Vsl	+3.22	±0.03v

Check all voltages for a ripple of less than 100 MV; settings refer to nominal conditions.

NOTE: The specification of the 48v power supply is 48 ±4.0v on machines with the revised Mid-Pac power supply (EC255055). The 24v power supply is combined with the 115v supply and has no specification for tolerance.

Timing waveforms and delays may be scoped at the following points. The Basic Clock is on ALD KC001; the T-Clock is on ALD KC041. Scope set-up: SYNC external on pin 01A-B1M6B03 (clock odd A); HORIZ 100ns/div; VERT lv/div; INPUT MODE DC. Scope points:

For the Basic Clock:

Clock odd	01A-B1M6	B03; D02; D05
Clock odd delayed	01A-B1B4	B03; D02; D05
Clock even	01A-B1M6	D09; B13; D12
Clock even delayed	01A-B1B4	D09; B13; D12

For the T-Clock:

+T1	01A-B1J6	B08
+T1 delayed	01A-B1D7	B07
+T2	01A-B1J7	D07
+T2 delayed	01A-B1J6	D07
+T3	01A-B1M7	D09
+T3 delayed	01A-B1C6	B07
+T4	01A-B1M7	B08
+T4 delayed	01A-B1B5	B10

Clock timings are shown in Figure 53; circuits conditioned by the T-Clock are shown in Figure 54.

TROS

Current Adjustment

NOTE: With the select voltage switch in the ROS position, the internal CE panel meter is connected across a resistor to measure the voltage drop (ALD PA820; YC157 for Mid-Pac supplies). The meter scale is marked to give a reading in milliamps for the voltage drop.

Adjust the TROS current using the marginal checking procedure, as follows:

1. Press system reset.
2. Set the select voltage switch (on the internal CE panel) to ROS position. Check TROS drive current for 66 milliamps nominal.
3. Load external diagnostic 43C2. This diagnostic exercises TROS words.
4. Run the diagnostics for one minute at nominal current.
5. Vary TROS current ±20 percent from nominal. The diagnostic must run without error for 2 minutes on each margin.
6. Press system reset to stop the test.

If the test fails to run at either margin, note the plus and minus limits where the test will run without error. The plus limit should not exceed 90 ma. Adjust the current to the midpoint of the plus and minus limits and repeat steps 5 and 6. Current above 66 ma is excessive and may cause intermittent problems.

TROS Timing

Normally, you should not adjust timing of TROS in the field. However, if a timing card is replaced (Figures 57, 57.2), insert the new card into the board in place of the old one and, if timing is necessary, follow the sequence given in Figures 55-58.1.

TROS units may have one of two types of timing cards or a combination of the two. However, the part numbers are the same. The cards may be identified by checking with the delay line layout in Figures 57 and 57.1, or by the EC levels as shown in Figure 57.1. The alpha portion of the EC number is stamped on the base of the SLT cards.

Figure 57 illustrates delay line plugging of early type cards. Figure 57.1 shows how to plug the current delays and also shows initial settings so the cards can function properly in any 2040 TROS unit. If a later type card replaces an earlier type, plug it as shown in

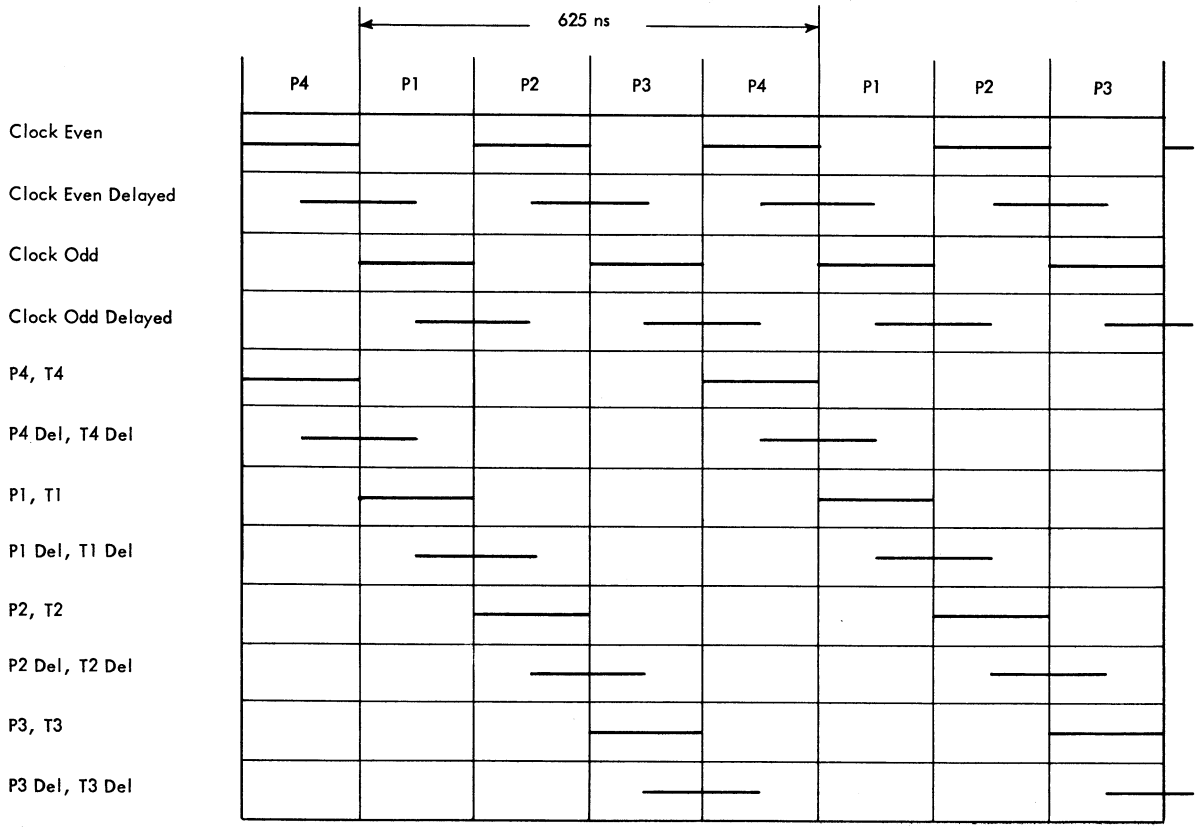


Figure 53. Clock Timing

T1

Decode Sense Latches
ROAR to ROBAR
Reset P, Q and R
Set P, Q, and R
Reset B Ctrl Latches
Set B Ctrl Latches
Set LSAR
Reset LSAR
Reset Q Switch
Set Skew
Reset Function Reg
Set Function Reg
Set I/O or CPU Mode

T2

Decode Sense Latches
Select Main Storage
Set ROAR
Reset ROAR
Reset Condition Bits
Set Condition Bits
Select Local Storage SPLS

T3

Decode Sense Latches
Reset A, B, C, D
Regs on 9 and 18 Bit Transfer
Inhibit Call Read Only Storage
Reset H, J
Set Stats, Reset Stats
Set H, J, A, B, C, D Regs
Set Carry Latch

T4

Reset Sense Latches
Test for Trap
Reset External Interrupts on Q Bus Sample
Inhibit Call Read Only Storage
Reset Skew Buffer

T1 DEL

Select Local Storage
Set LSAR
Set P, Q and R
Set B Ctrl Latches
Set Skew Reg
Set Function Reg
Sample of ISA

T2 DEL

Set ROAR
Set Condition Bits
Early Conditions Available
Early Checks:
R, P, Q Sense
Latch Parity Decoder
LSAR
ROBAR

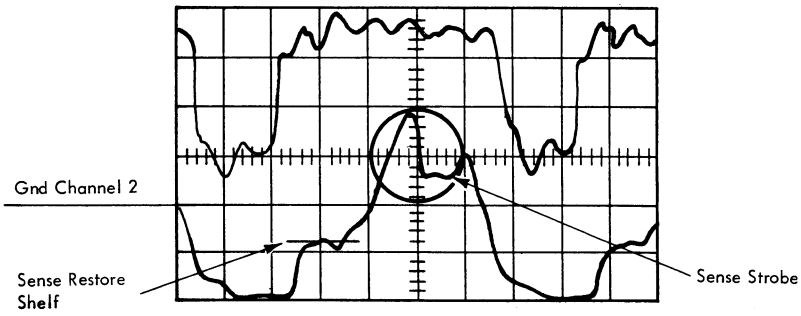
T3 DEL

Set H, J from LSAR
Set Stats
Local Storage Output
ALU Output
Set A, B, C, D, H, J from R Reg
Set D from Main Storage
Inhibit Change to P and Q
Set Channel Interrupt Latches
Set Dump
Inhibit Function Reg Change
Set Carry Latch

T4 DEL

Sense Latch Output Active
Decode Sense Latches
Late Checks:
ALU 2 Wire
Stack Output

Figure 54. Circuits Conditioned by "T" Clock



Sweep Speed 100ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1N5D11	EC 311
Channel 1 2v/cm	Clock Pulse	A1G6D05 6K A1H6D05 8K	EC 231
Channel 2 1v/cm	Sense Amp Output Bit 0	A2D2B05 6K A2E2B05 8K	EB 011

Figure 54.1 Quick Timing Check (Recording Obtained Using Tektronix Type 453 Scope)

Figure 57.1. In any case, timing must be thoroughly checked after replacing timing cards.

Set power supplies at normal before timing is checked. When a timing card is changed, check the timing pulses on the new card after setting them to the same delays as those plugged on the card it replaces (Figure 57). The sets of taps for each delay line are so arranged that when the card is viewed from the component side with the connector at the bottom, the sets of taps are numbered clockwise. If the card has only two delays, they may be located in positions 1 and 2, or in positions 3 and 4.

The pins are numbered 1 through 26 across the card. Pins have delays from 5ns to 50ns as shown. To change a delay, remove the connecting jumpers and replace the jumpers with a jumper connecting all 10 pins. To delay a pulse a given amount, cut the jumpers for the desired delay.

NOTE: Remove all intermediate pins for unwanted delays.

Quick Timing Check

For a quick check of TROS timing before any adjustments are made, set the scope according to Figure 54.1 and observe the "bat's ears" effect of one of the sense amplifier outputs (bit 0 shown). If the sense amplifier output has one peak rather than two, that is, if the level falls off after the first peak, check timing of the TROS unit.

All TROS lines in the following adjustments are on ALD pages EB041, EC231, EC241, EC251, and EC281. Perform the adjustments in the following sequence:

(Text locations in Figure 55 refer to machines with 8K TROS.)

1. Adjust front edge of sense restore amplifier (02A2G2J05) to fall at 90ns (±10).

2. Adjust the front edge of gate strobe timing (02A1H6J07) to fall at 205ns (±10).

3. Adjust the driver supply front edge (02A1H4D09) to fall between 205 and 310ns. The duration of the driver supply signal must be 205ns (−10).

4. Adjust the back of the sense restore amplifier (02A2G2J05) to rise at 230ns (±10).

5. Adjust delay line output A (02A1G6J12) to fall at 225ns (±10); the 50ns line must always be left in the circuit.

6. Adjust the front edge of the driver strobe (02A1H4D07) to rise at 300ns (±10); maintain 75ns (±10) separation between the fall of delay line output A and the rise of the driver strobe.

7. Adjust delay line output B (02A1K6J04) to fall at 275ns (±10); delay line output B must fall 25ns (±10) before driver strobe rises.

8. Adjust front edge of sense reset timing (02A1-K6J11 to rise at 340ns (±10); maintain 65ns (±10) separation between the fall of timing card B delay and the rise of sense reset; also maintain a minimum duration of 70ns for sense reset.

9. Adjust the front edge of sense strobe timing (02A1M6J05) to rise at 410ns (±10); maintain 135ns (±10) separation between the rise of this pulse and the fall of timing card B delay line; also maintain a minimum duration of 75ns for the sense strobe pulse.

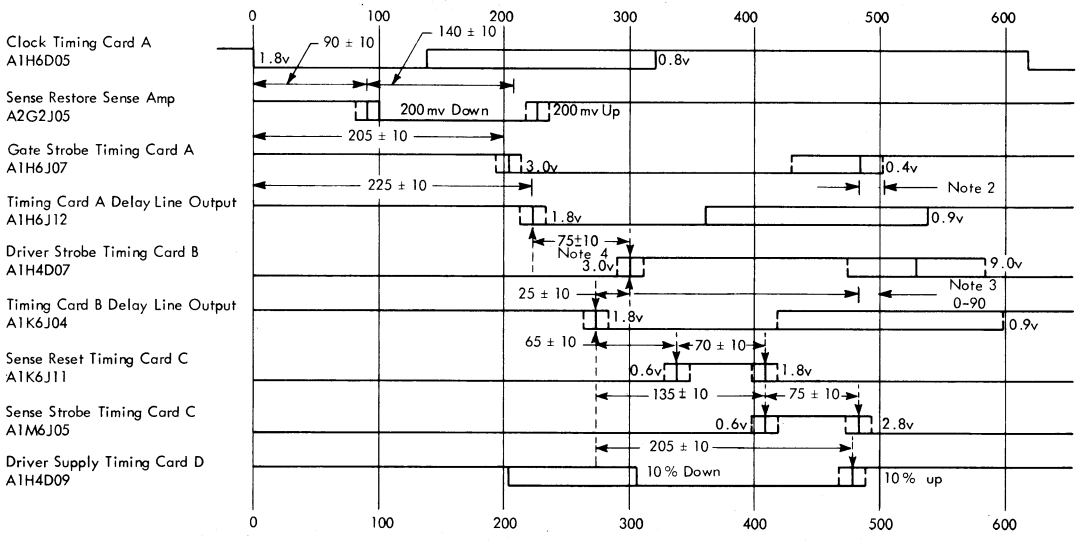
10. Adjust the back edge of sense reset (02A1K6J11) to fall at 410ns (±10); maintain 70ns minimum duration of the sense reset pulse.

Clock		Test Point Location			
		6K TROS	8K TROS	Name	Time in Nanoseconds
1	Card A Type 4365	02A2G2J05	02A2G2J05	Sense Restore, Front Edge	90 ± 10
2	A1G6 (6K) A1H6 (8K)	02A1G6J07	02A1H6J07	Gate Strobe, Front Edge	205 ± 10
		02A1G4D09	02A1H4D09	Driver Supply, Front Edge	205-310
3		02A2G2J05	02A2G2J05	Sense Restore, Back Edge	230 ± 10
4		02A1G6J12	02A1H6J12	Delay Line Output A, Front Edge	225 ± 10
1	Card B Type 4366	02A1G4D07	02A1H4D07	Driver Strobe, Front Edge	300 ± 10
2	A1J6 (6K) A1K6 (8K)	02A1J6J04	02A1K6J04	Delay Line Output B, Front Edge	275 ± 10
1	Card C Type 6133	02A1J6J11	02A1K6J11	Sense Reset, Front Edge	340 ± 10
2		02A1L6J05	02A1M6J05*	Sense Strobe, Front Edge	410 ± 10
3		02A1J6J11	02A1K6J11	Sense Reset, Back Edge	410 ± 10
4	A1L6 (6K)	02A1L6J05	02A1M6J05*	Sense Strobe, Back Edge	485 ± 10
	A1M6 (8K)	02A1G6J07	02A1H6J07	Gate Strobe, Back Edge	485 +20, -55
	A1K4 (*)	02A1G4D07	02A1H4D07	Driver Strobe, Back Edge	530 ± 55
1	Card D Type 4333				
2	A1G4 (6K) A1H4 (8K)	02A1G4D09	02A1G4D09	Driver Supply, Back Edge	480 ± 10

* M6 locations are moved to K4 on machines with 8K TROS at EC256852 or later.

Timing sequence is top to bottom.

Figure 55. TROS Timing Locations and Sequence of Adjustment



Notes:

1. All timing measurements are made at the voltage point referenced on each pulse and all are referenced from ground except sense restore and driver supply, which are indicated.
2. Gate strobe back edge originates from timing card C and is not tuned. It should occur -20 to -55 nanoseconds with respect to sense strobe back edge, after all timing is set up.
3. Back edge of driver strobe is not tuned. It should occur 0-90 nanoseconds after sense strobe back edge, after all timing is set up.
4. After all timings are made, double check driver strobe to ensure it falls withing 300 ± 10 nanoseconds after clock at the indicated level.

Figure 56. TROS Internal Timing

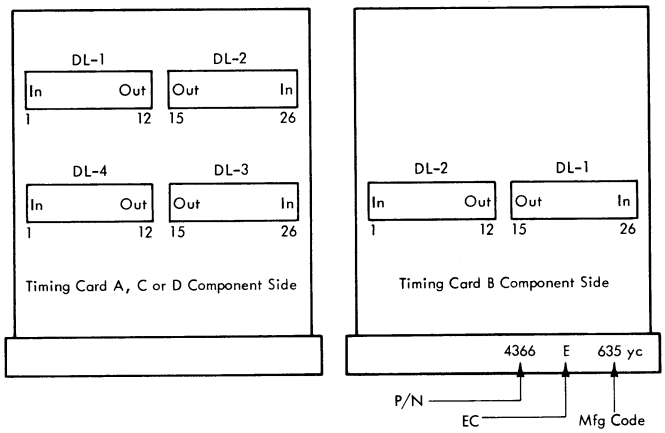


Figure 57. Timing Cards — Early Type

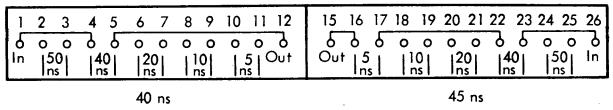


Figure 57.1. Example for Plugging Early Type Timing Cards

11. Adjust the back edge of sense strobe to fall at 485ns (±10); maintain 75ns minimum duration of the sense strobe pulse.

12. Adjust the back edge of gate strobe (02A1H6J07) to rise at 485ns (+20, −55).

13. Adjust the back edge of the driver strobe (02A1H4D07) to fall at 530ns (±55).

14. Adjust the back edge of the driver supply (02A1G4D09) to rise at 480 (±10); maintain 205ns (−10) separation between the rise of the driver supply pulse and the fall of timing card B delay.

The input/output timing should be as shown in Figure 58. To check that the ROS address bits are good prior to the driver strobe rise time (02A1H4D07), cycle CPU checkout (diagnostic control switch on CPU) and check any TROS address in CPU checkout.

Tape Deck Assembly Changing

Removal Procedure

For modules 8 to 15 go to the internal CE panel side of the frame. For modules 0 to 7 go to the right side. To remove the tape deck assembly:

1. Loosen the bottom screws on the cover assembly.
2. Remove the top screws, and slide the cover upwards and outwards. The cover slides off the bottom screws and can be removed.
3. Select the tape deck assembly to be changed. Modules 7 and 15 are nearest the main console.
4. Loosen the top and bottom retaining screws.
5. Unplug the two connectors to item 14 and gently fold them over the sides (Figure 62).
6. Hold the assembly with one hand and remove the two retaining screws.
7. The assembly can now be lifted out for inspection. To install the module, reverse the procedure.

Sense Winding and I Core Assembly Changing

Removal Procedure

First remove the tape deck assembly as previously described; then:

1. Select the assembly to be changed.
2. Unsolder the sense tags from the common strip tags. Spread the sense tag and common strip during the unsoldering operation. To resolder, hold the tip of the tags together with a pair of long-nose pliers.
3. Using a small screwdriver, carefully push the assembly out from sense tag side. Do not damage sense windings with screwdriver.

Replacement Procedure

NOTE: Be sure the sense and commoning strip tags are straight, clean, and properly tinned.

1. Insert the assembly so that the sense tags go below the respective sense commoning strips.
2. Solder the sense tags to the commoning strip tags by holding the tags together (with pliers or tweezers) near the commoning strip. Take care not to apply excessive heat or the commoning strip tag connections may be damaged.

Tape Changing

Removal Procedure

Refer to Figures 62 and 63.

First remove the tape deck assembly as previously described and place it on a flat work surface. Unplug the tape to be removed. If a tape numbered between 00 and 63 is to be removed, omit steps 1 and 2. If a tape numbered between 64 and 127 is to be removed, follow steps 1 and 2.

1. Unscrew the two retaining screws and remove the U-core retaining plate. (This plate is positioned over the tapes and holds the U cores in position.)
2. Remove the U cores by hand. Do not invert the assembly to remove the cores as this practice may damage them.
3. Remove the upper tape assembly retaining screw and loosen the bottom retaining screw.
4. Locate the tape to be changed. Remove the bottom retaining screw (i.e., bottom of the module as it is installed in the gate). Insert the retaining screw from the bottom of the module through the tapes (in the direction that the U cores were inserted) that are not to be changed.
5. Remove the selected tape.

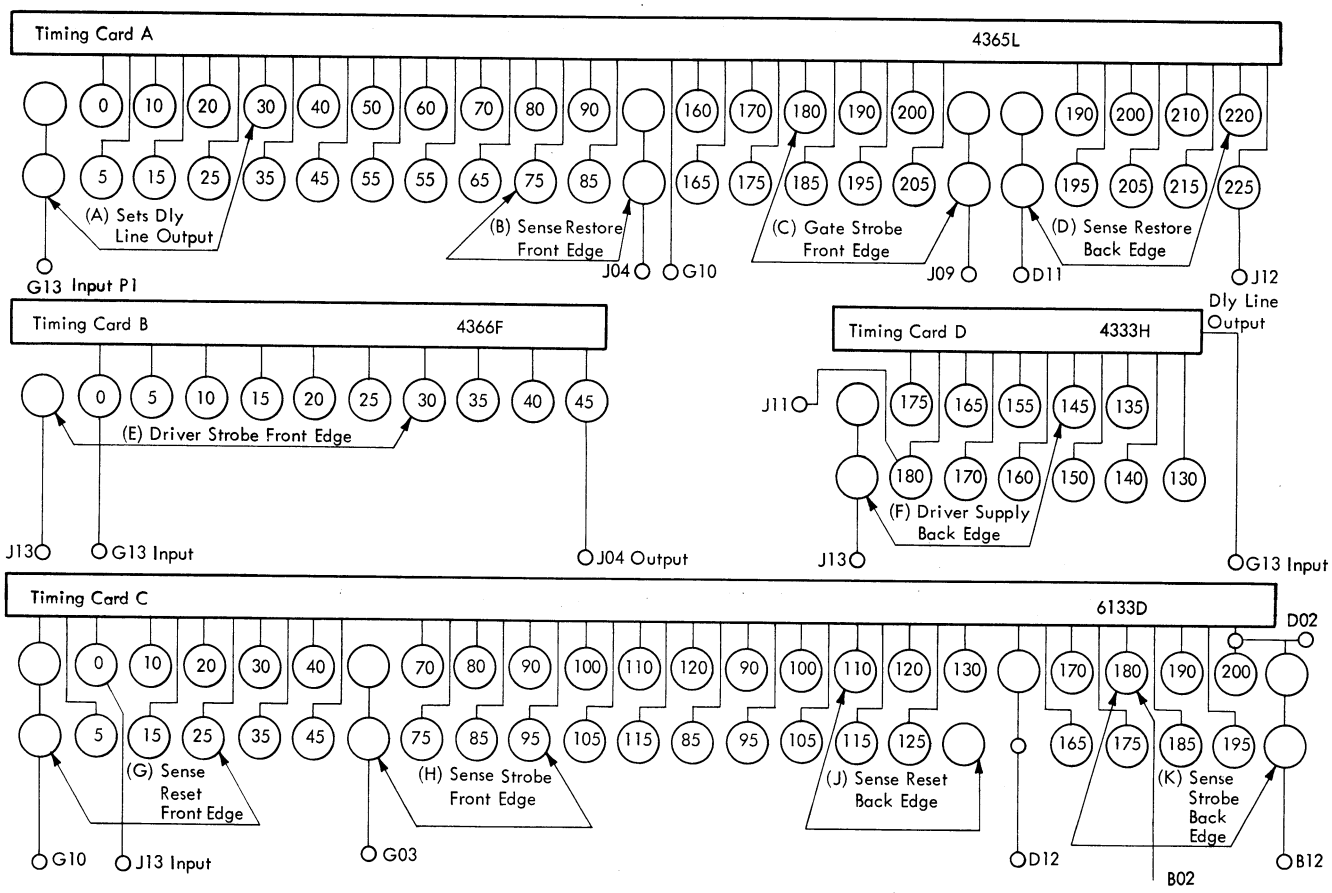
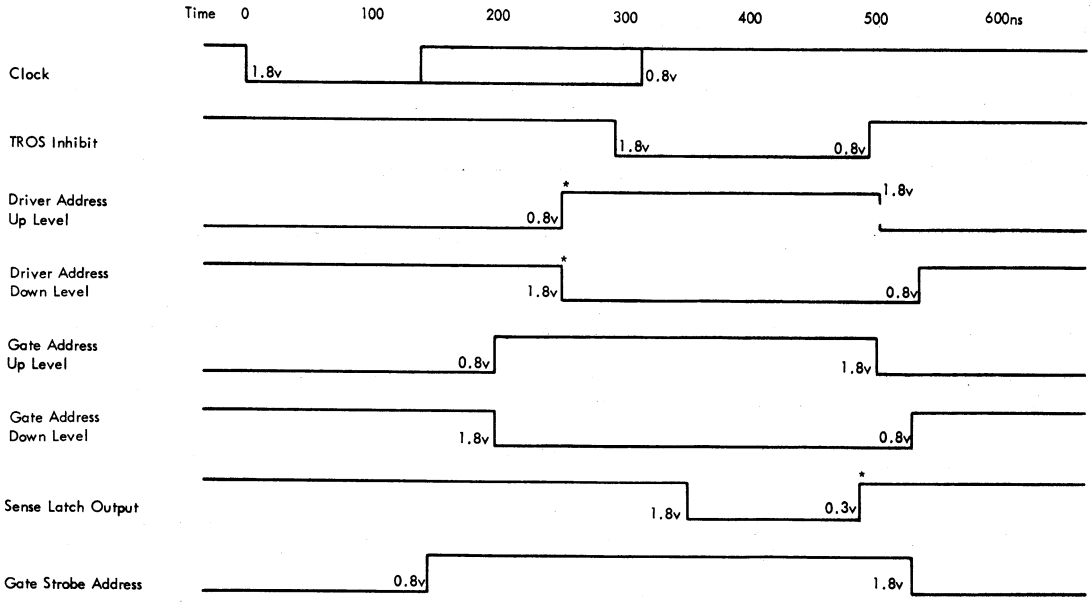
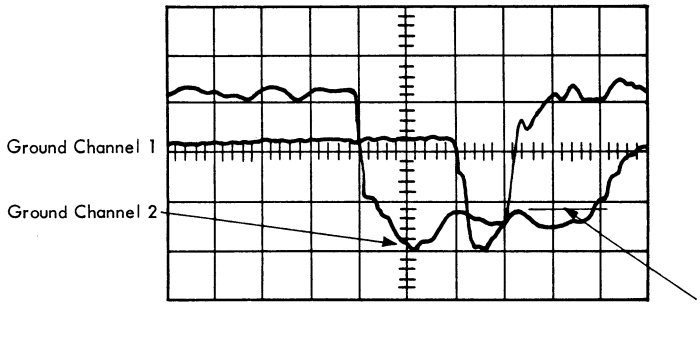


Figure 57.2. Present Timing Cards

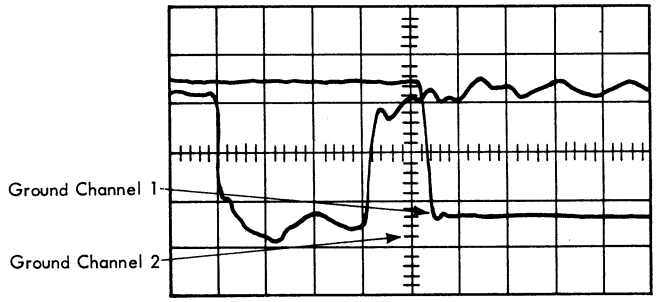


*These timings vary with drive strobe timing front edge (T) (shown at 300ns).

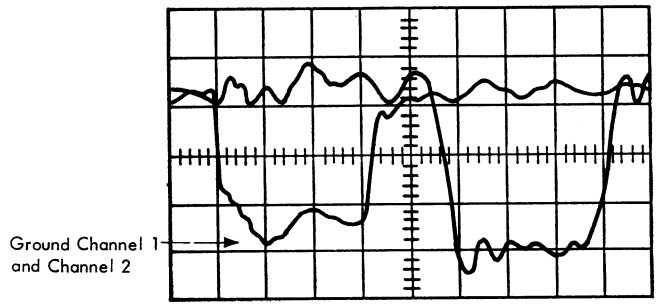
Figure 58. Input/Output Timing



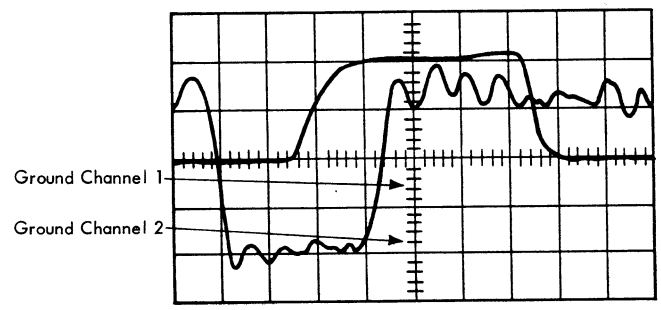
Sweep Speed 50 ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 2 1v/cm	-Clock Pulse	A1 G6 D05 (6K) A1 H6 D05 (8K)	EC 231
Channel 1 1v/cm	Sense Restore	A2G2J05	EB 041



Sweep Speed 50ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 2 1v/cm	-Clock Pulse	A1 G6 D05 (6K) A1 H6 D05 (8K)	EC 231
Channel 1 2v/cm	Gate Strobe	A1H6J07 (6K) A1G6J07 (8K)	EC 231

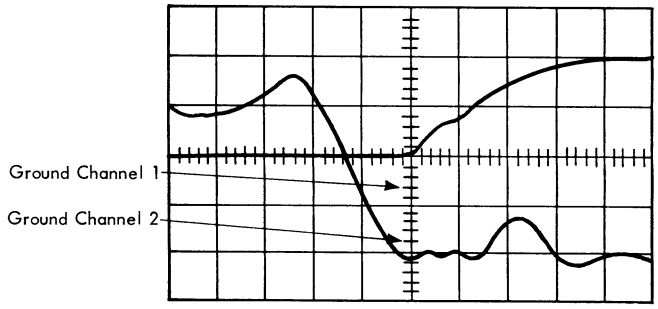


Sweep Speed 50ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 2 1v/cm	-Clock Pulse	A1 G6 D05 (6K) A1 H6 D05 (8K)	EC 231
Channel 1 1v/cm	Delay Line Output A	A1H6J12 (8K) A1G6J12 (6K)	EC 231

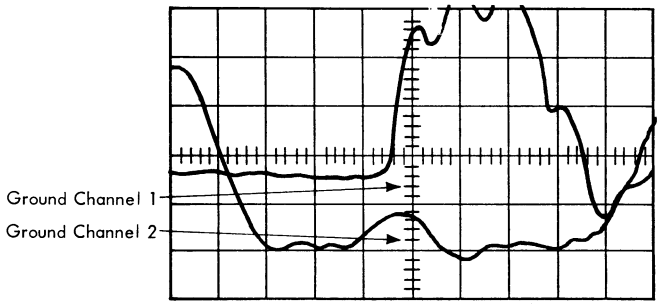


Sweep Speed 50ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 2 1v/cm	Delay Line Output A	A1H6J12 (8K) A1G6J12 (6K)	EC 231
Channel 1 5v/cm	Driver Strobe	A1H4D07 (8K) A1G4D07 (6K)	EC 281

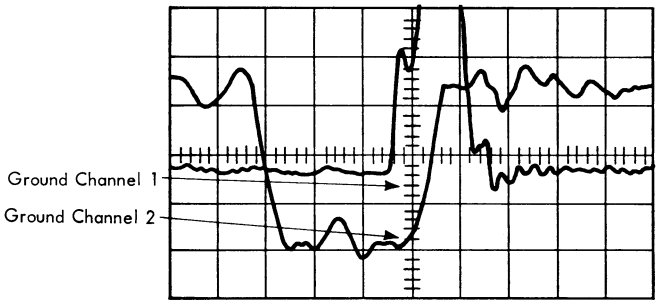
Figure 58.1. TROS Timing – Scope Traces (Sheet 1 of 2)
(Recordings Obtained Using Tektronix Type 453 Scope)



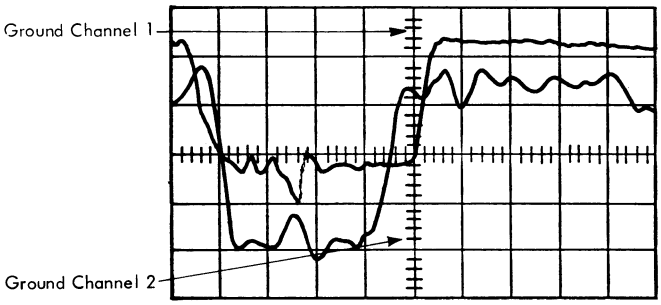
Sweep Speed 20ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 1 5v/cm	Driver Strobe	A1H4D07 (8K) A1G4D07 (6K)	EC 281
Channel 2 1v/cm	Delay Line Output B	A1K6J04 (8K) A1J6J04 (6K)	EC 241



Sweep Speed 20ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 2 1v/cm	Delay Line Output B	A1K6J04 (8K) A1J6J04 (6K)	EC 241
Channel 1 1v/cm	Sense Reset	A1K6J11 (8K) A1J6J11 (6K)	EC 241



Sweep Speed 50ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 1 1v/cm	Delay Line Output B	A1K6J04 (8K) A1J6J04 (6K)	EC 241
Channel 2 1v/cm	Sense Strobe	A1K4J05 (8K) A1L6J05 (6K)	EC 251



Sweep Speed 50ns/cm	Name	Test Point	ALD Page
Sync Pulse	-Clock Pulse	A1 N5 D11	EC 311
Channel 2 1v/cm	Delay Line Output B	A1K6J04 (8K) A1J6J04 (6K)	EC 241
Channel 1 500 mv/cm	Driver Current Monitor Point	A1H4D09 (8K) A1G4D09 (6K)	EC 281

Figure 58.1. TROS Timing – Scope Traces (Sheet 2 of 2)
(Recordings Obtained Using Tektronix Type 453 Scope)

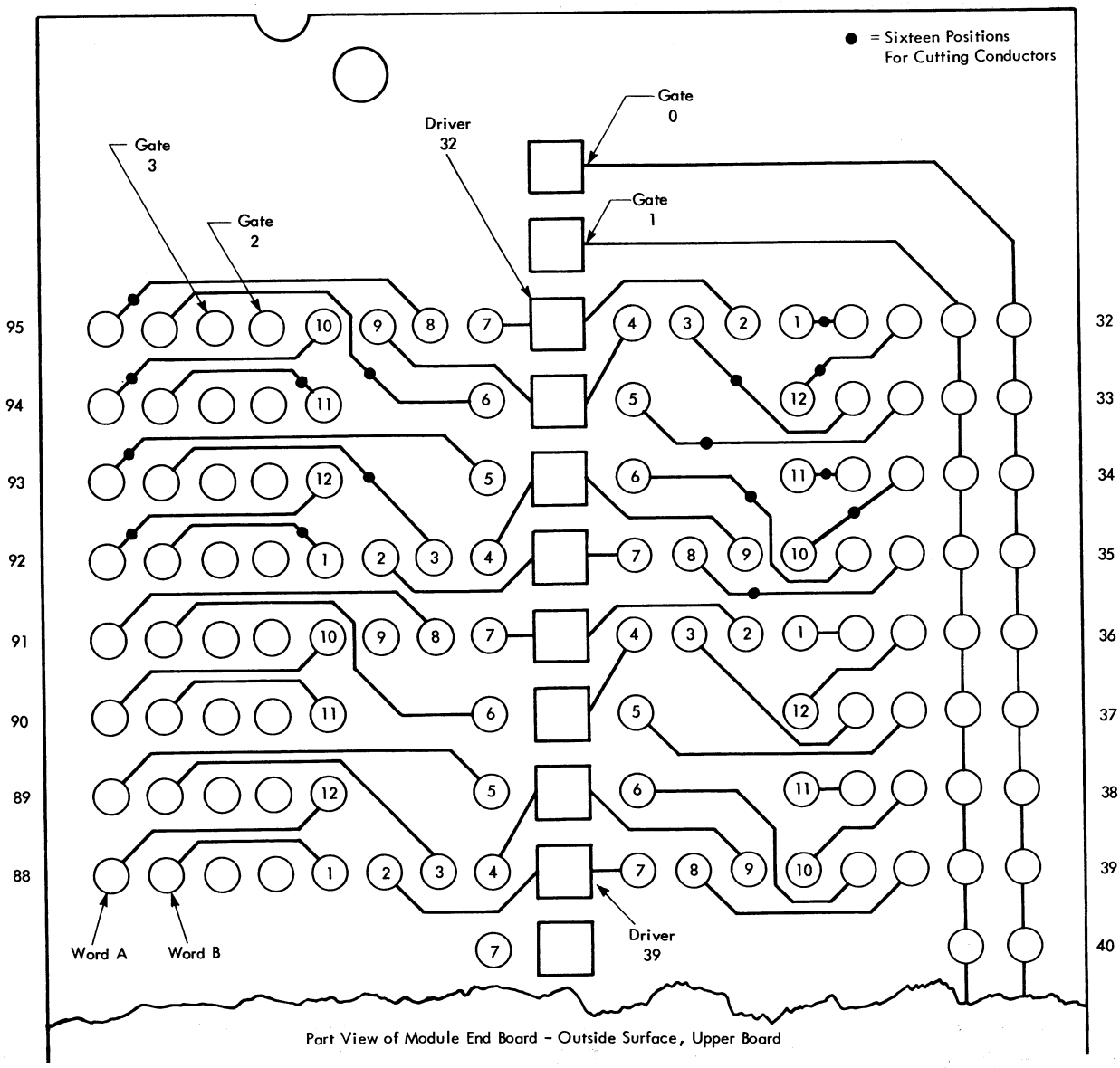


Figure 59. Cutting Conductors, TROS Module End Board

Replacements

1. Insert the replacement tape at the correct position within the tape group.
2. Remove the bottom screw from the module, reposition the tapes, and insert the bottom screw correctly.
3. Check the replacement tape for continuity, using the two outside and the two inside pins.
4. Tighten the tape locating screws and insert the U cores.
5. Attach the core retainer.
6. Relocate the four tape terminal pins. When inserting the terminal pins, *make sure* that they are positioned at 90 degrees to the assembly card surface to prevent fouling in the socket.

Replace the tape deck assembly by reversing the procedure previously described under "Removal Procedure" (Tape Deck Assembly Changing).

Diode Changing

TROS diodes are mounted as FDD (four double diode) substrates (SLT module), on the inside of the two boards on the top end of each TROS module. Each module has two end boards and each end board has 16 substrates. Each substrate has eight diodes. This gives 256 diodes per module – one for each word, two for each tape. For end board layout and diode wiring, refer to Figure 61. Locate the substrate holding the faulty diode and the pins across which it is connected. Refer to Figure 59 to see where the various land patterns should be cut.

1. Draw the engraving tool across the land pattern to cut it. Cut the land pattern in two places so a small portion of it may be removed.

2. Between the relevant word tape termination pin and C or Z tape termination pin, solder the replacement diode (Part 2414895) using the detail shown in Figure 60. Be sure the polarities of the mounted diodes are correct.

3. Insulate the diode leads and fit the diode close to the board. Make mechanically sound joints before soldering.

Locating an Open Diode or Open Tape

A no-output condition from the sense latches may be caused by an open diode or an open tape drive line.

1. Analyze failing ROS address to determine which module is affected.

2. Use the tape location template PN 5352274 (Figure 60.1) to determine the physical location of the defective diode or tape.

3. Use an ohmmeter to determine whether a diode or a tape is defective.

4. Replace the defective part by following the change procedures outlined in this section of the manual.

Local Storage

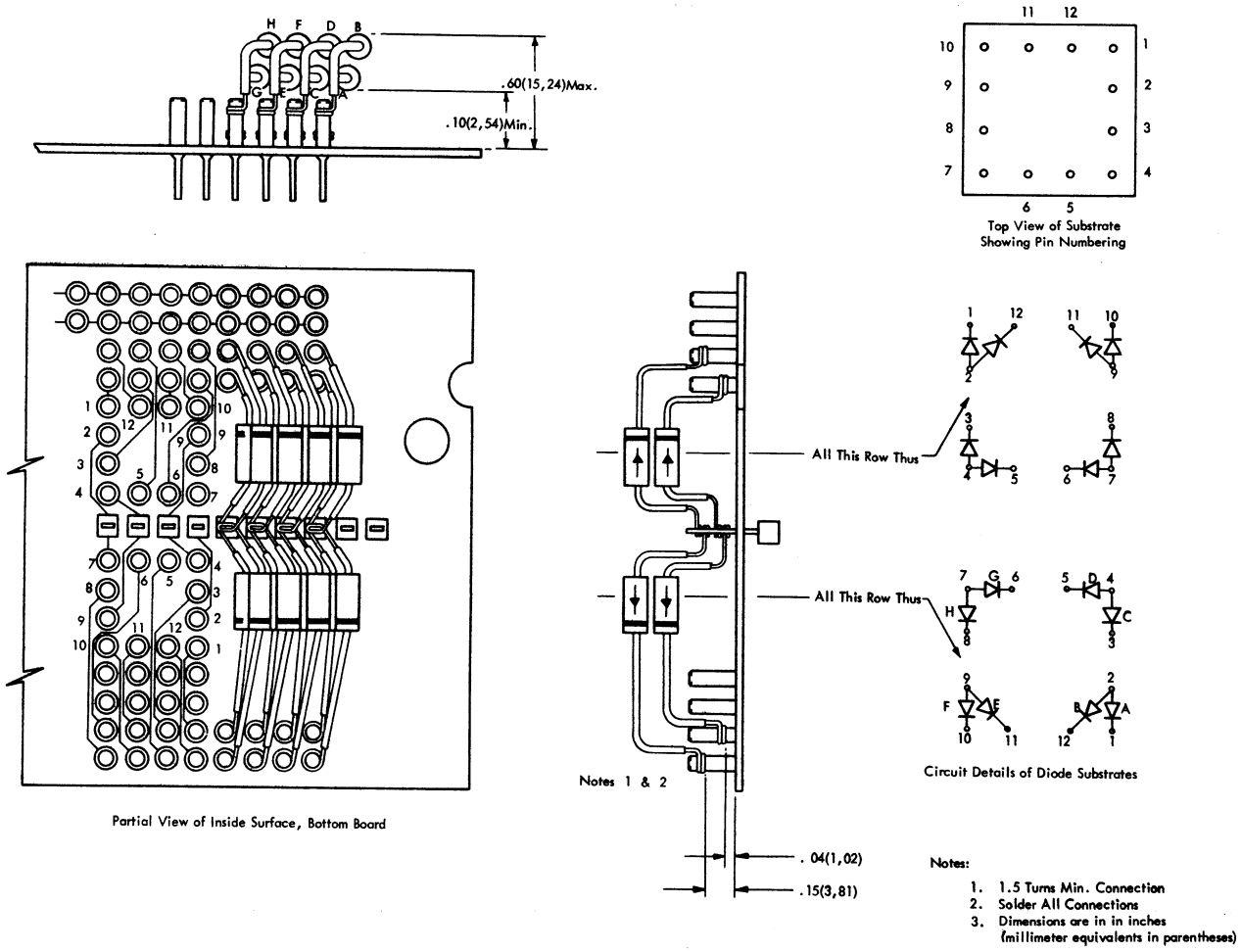
Voltage Adjustment

This procedure tests that the local storage unit operates correctly when the voltage is biased ±6 percent. It is used for installation and preventive maintenance.

Marginal Check

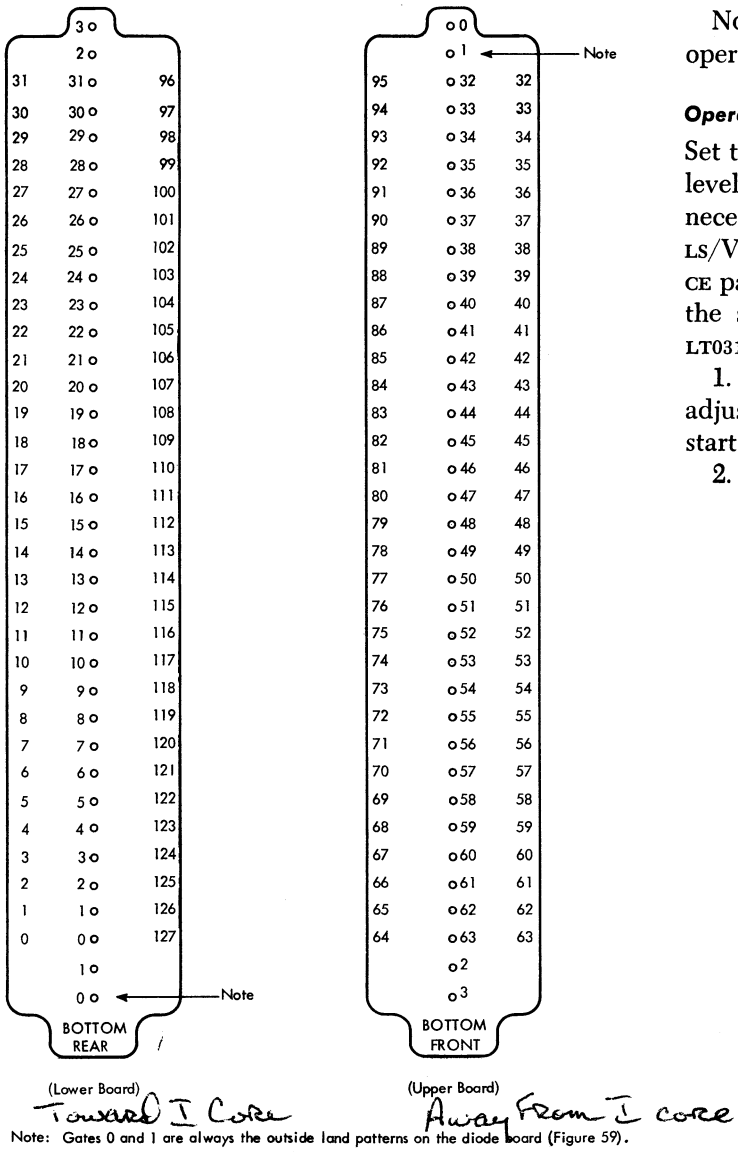
1. Set the diagnostic control switch to local storage pattern and run the test. Record the nominal voltage (present setting).

2. Vary LS/Vxy and LS/Vm (on the internal CE panel) one voltage at a time, ±6 percent from nominal. The pattern test must run for one minute without errors on each margin. If the test fails to run, the local storage operating point voltage should be checked using the procedure in the following section.



Partial View of Inside Surface, Bottom Board

Figure 60. Diode Soldering



Note: Gates 0 and 1 are always the outside land patterns on the diode board (Figure 59).

Figure 60.1. TROS Tape Location Template, Part 5352274

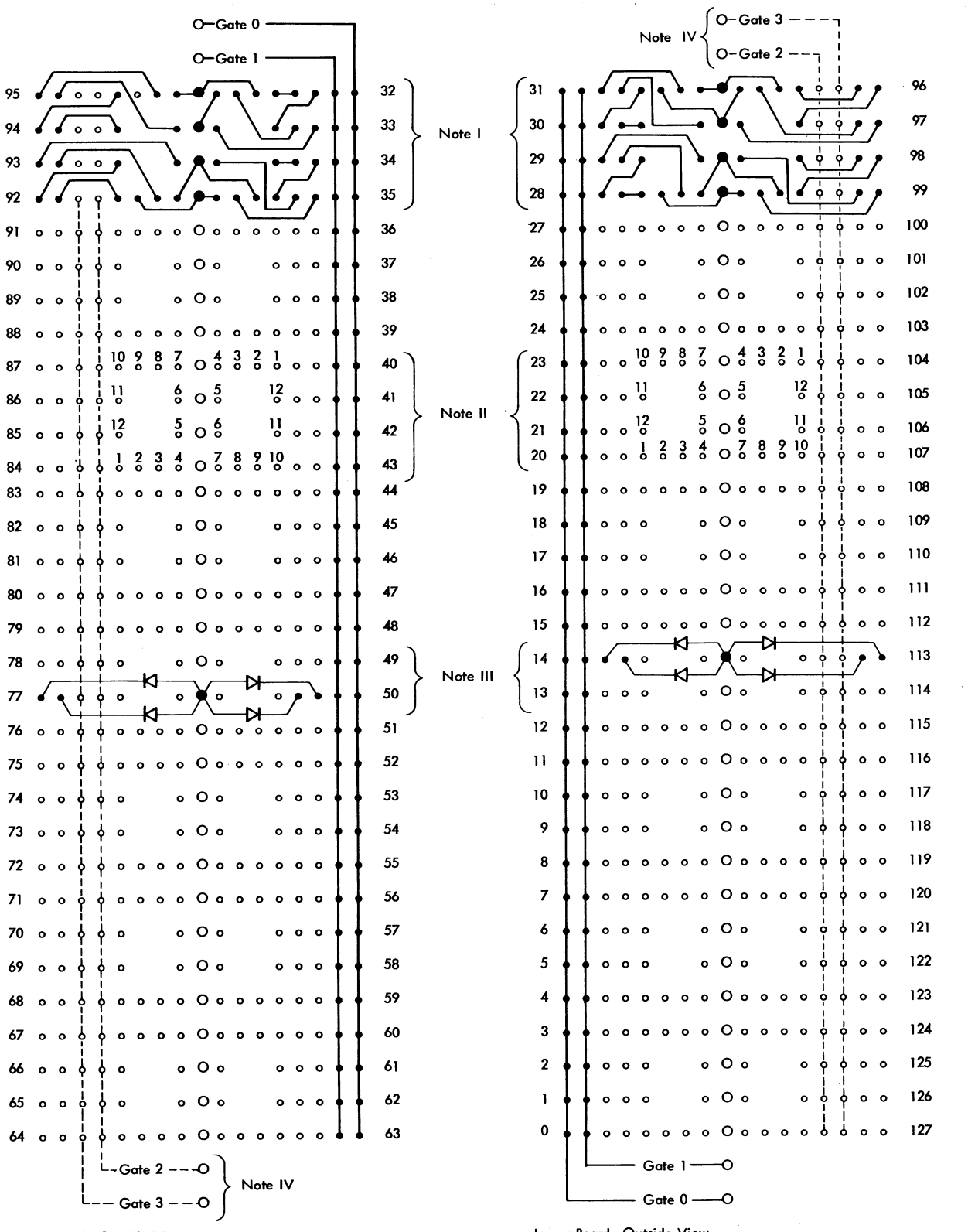
NOTE: If marginal checking gives errors after the operating point voltage adjustment, check for a cause.

Operating Point Voltage Adjustment

Set the logic voltages +6, +3, and −3v to the correct levels. Initial adjustments on three potentiometers are necessary to optimize local storage performance. The LS/Vm and LS/Vxy potentiometers are on the internal CE panel. The LS/Vsl (sense level) potentiometer is on the SLT card at 01A-D1B4. The circuitry is on ALD LT031.

1. Run the local storage pattern test while doing the adjustment. Each time errors stop the machine, restart the test.
2. At 77 degrees F (25 degrees C), set LS/Vm to

↑
IF Room Temp 70°



Upper Board, Outside View

Lower Board, Outside View

Note I: Land patterns shown here are repeated for each FDD pair on the board.

Note II: FDD (four double diode) modules are mounted on the inside of the boards; pin numbers shown represent pin numbering for all modules on the board.

Note III: Replacement diodes should be wired as shown.

Note IV: Dotted lines show land patterns located on the inside of the board.

Figure 61. Module End Boards

1. Rod
2. Block
3. Carrier
4. 'I' Core
5. Spring
6. Strip
7. Chassis
8. Support
9. Rail
10. Diode Board
11. FDD Substrate
12. I/O Cables
13. I/O Cables
14. I/O Cable Card
15. Cable Clamp
16. Terminating Pins
17. Clamp
18. Tape Stack
19. Tape Stack
20. Alignment Pin
21. 2 Banks of 30 'U' Cores
22. Retainer
23. Insulator
24. Dummy Carrier

(#) = Tape Number

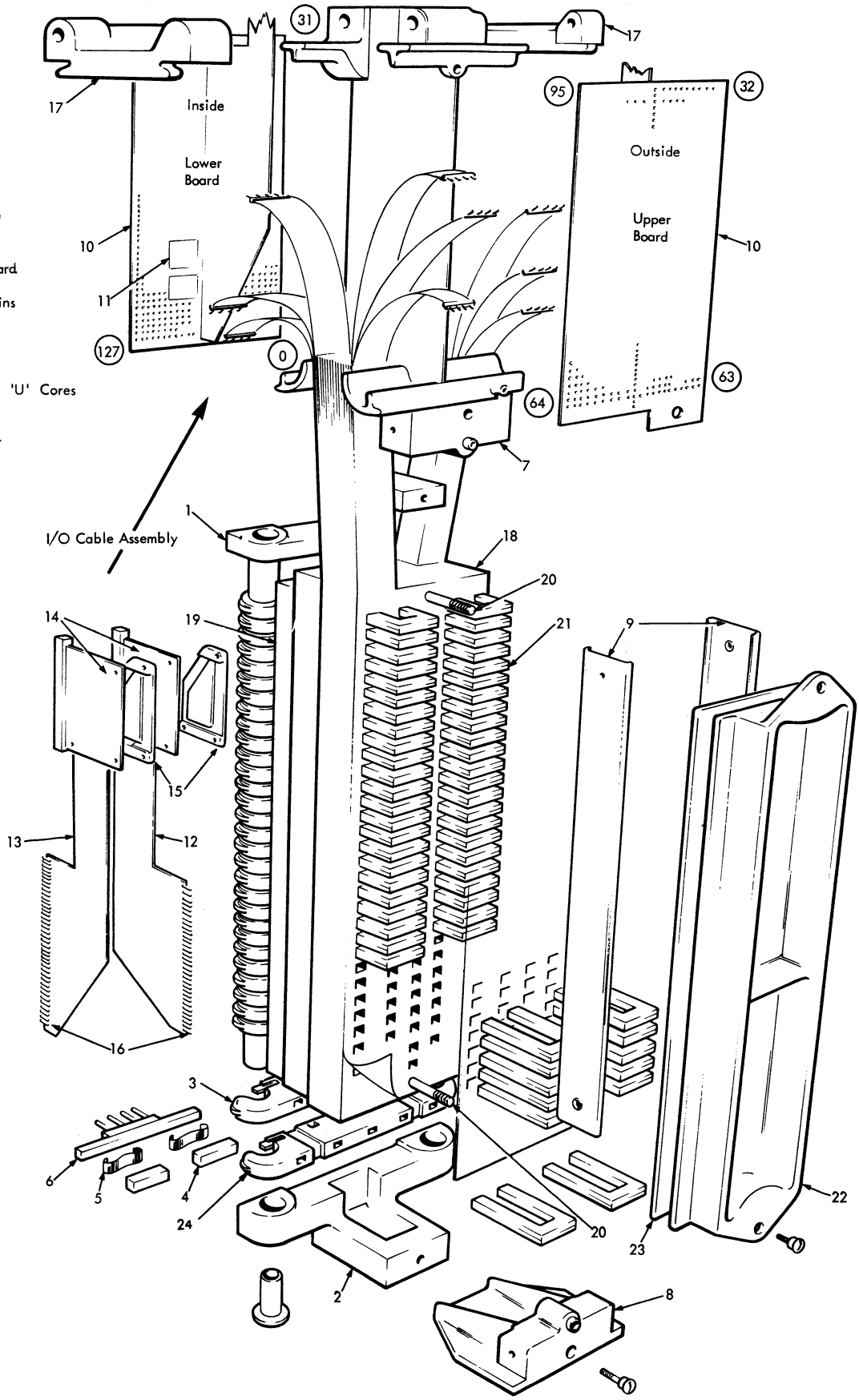


Figure 62. TROS Module (Exploded View)

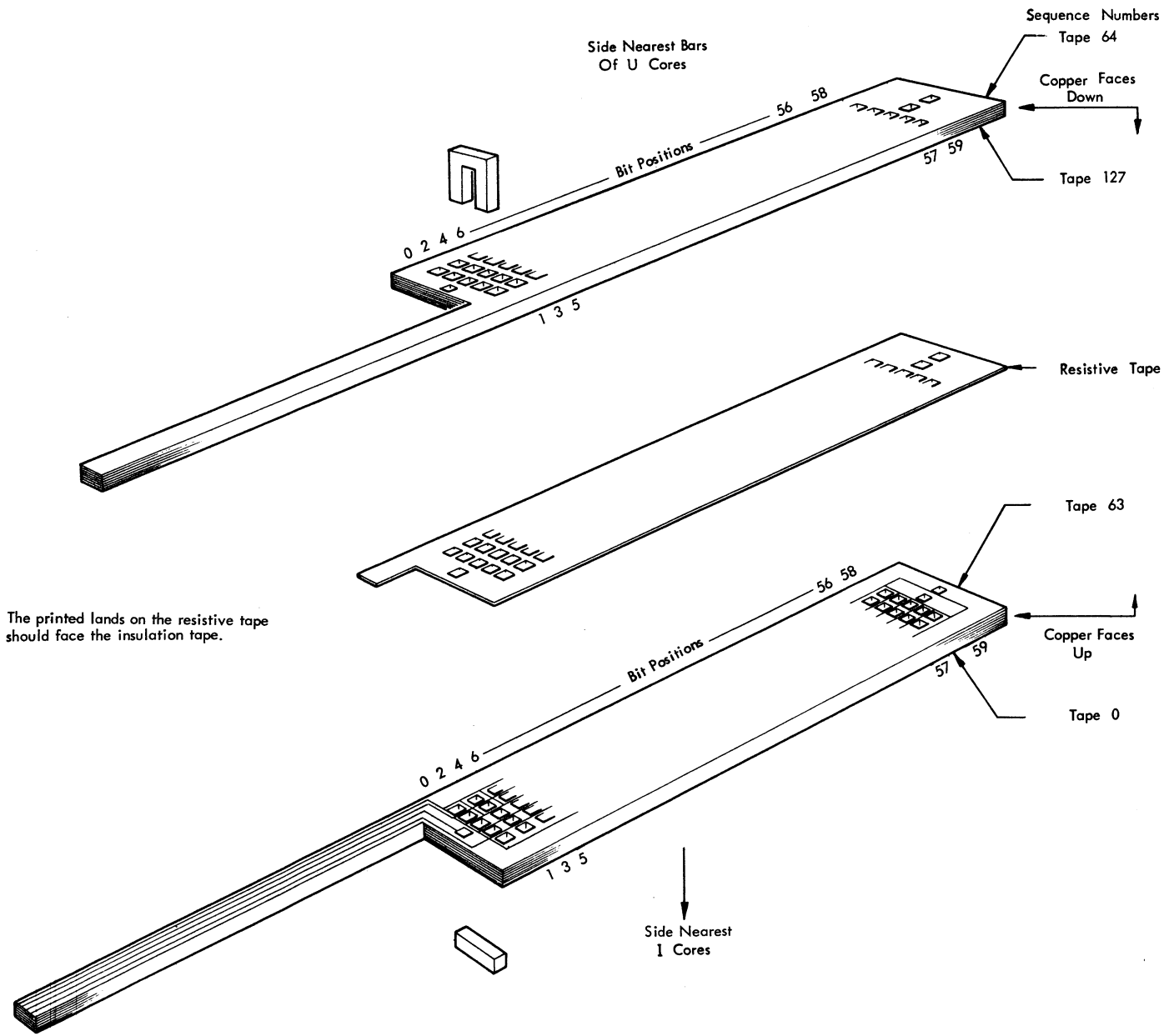


Figure 63. Tape Numbering and Arrangement

List Of Tapes Shown In Order Of Stacking

Tape Stagger A	Tape Stagger B	Tape Stagger C
	64	65
66	67	68
69	70	71
72	73	74
75	76	77
78	79	80
81	82	83
84	85	86
87	88	89
90	91	92
93	94	95
96	97	98
99	100	101
102	103	104
105	106	107
108	109	110
111	112	113
114	115	116
117	118	119
120	121	122
123	124	125
126	127	

Resistive Tape 14 - 1425

63		
60	61	62
57	58	59
54	55	56
51	52	53
48	49	50
45	46	47
42	43	44
39	40	41
36	37	38
33	34	35
30	31	32
27	28	29
24	25	26
21	22	23
18	19	20
15	16	17
12	13	14
9	10	11
6	7	8
3	4	5
0	1	2

−6.95v ±1 percent. For any other temperature set LS/Vm as shown on the tracking diagram (Figure 64). (The local storage temperature will be 7 degrees F higher than room temperature.) Measure the voltage between pin 01A-D1B6B05 and logic ground (any D08 pin) or with CE panel meter.

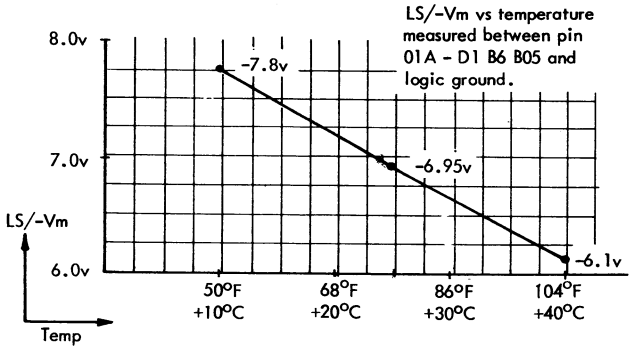


Figure 64. Local Storage Tracking (LS/Vm)

3. At 77 degrees F (25 degrees C), set LS/Vsl to +3.22 ±1 percent (Figure 66). Measure between pin 01A-D1B4B07 and logic ground.

4. Decrease LS/Vxy until the first error occurs and record this value. Measure between pin 01A-D1B4D09 and logic ground.

5. Restart the test and increase LS/Vxy until the first error occurs. Record this value.

6. Set LS/Vxy halfway between these two limits. The setting should be within ±0.3v from normal. The normal voltage is defined as the graph point ±4 percent at 25 degrees C (±2 degrees).

7. Decrease LS/Vsl until an error occurs, noting the LS/Vsl (lower limit).

8. Restart the local storage pattern test and increase LS/Vsl to the first error point (upper limit). The LS/Vsl swing should be 0.45v between the upper and lower limits at 25 degrees C (±2 degrees).

9. Set LS/Vsl 0.20v lower than the upper limit. It should be near midpoint at 77 degrees F (25 degrees C) and within ±4 percent of the reference value shown in Figure 66 at any temperature.

10. After performing the above adjustments, perform the steps in "Marginal Check."

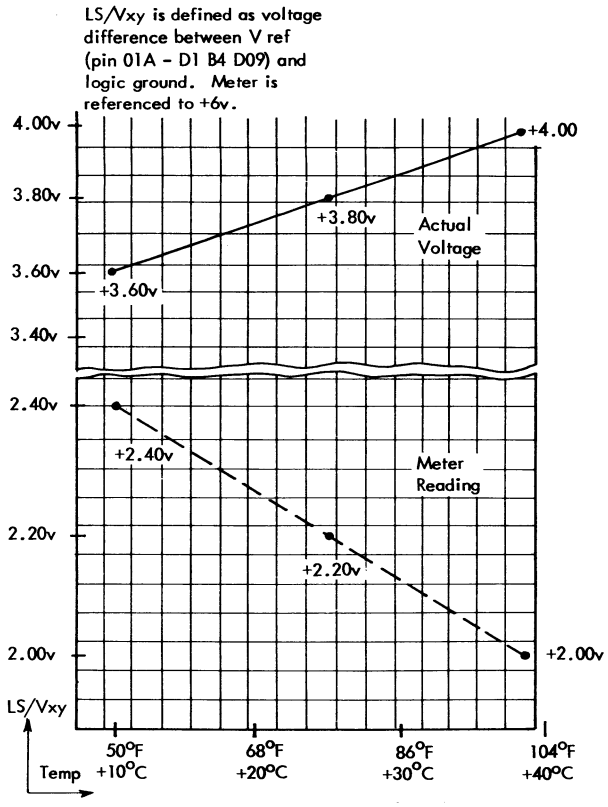


Figure 65. Local Storage Tracking (LS/Vxy)

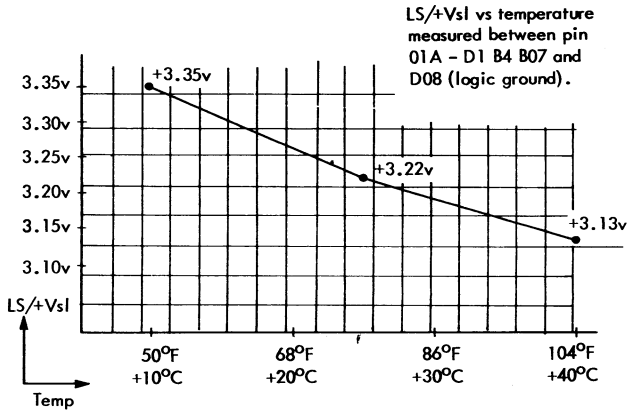


Figure 66. Local Storage Tracking (LS/Vsl)

Local Storage Delay Line Tap

One 50-nanosecond tap delay line is used for local storage timing. The card that holds the delay line is located at 01A-D1B2 (ALD LT011). Figure 67 shows the delay line tap pin numbers and the strobe set for a 150-nanosecond delay. Waveforms in Figure 67.1 show local storage control lines.

Array Changing

Removal Procedure

If any local storage core plane becomes defective, one of two SLT (4-72) cards must be changed. Local storage is mounted on two cards, each holding 144 twelve-bit words, 20 diodes, and one thermistor. This gives a total storage of 144 twenty-four bit words. The cards are located at 01A-D1D3 and 01A-D1E3. For core faults, the whole SLT card concerned must be changed (LT071).

CAUTION

The SLT core plane cards, though similar, are not interchangeable.

To change any one core plane card, first disconnect the two flat cable connectors, which are connected between the two cards, then extract and change the defective card.

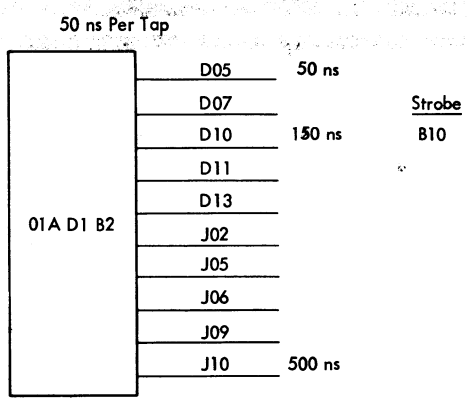
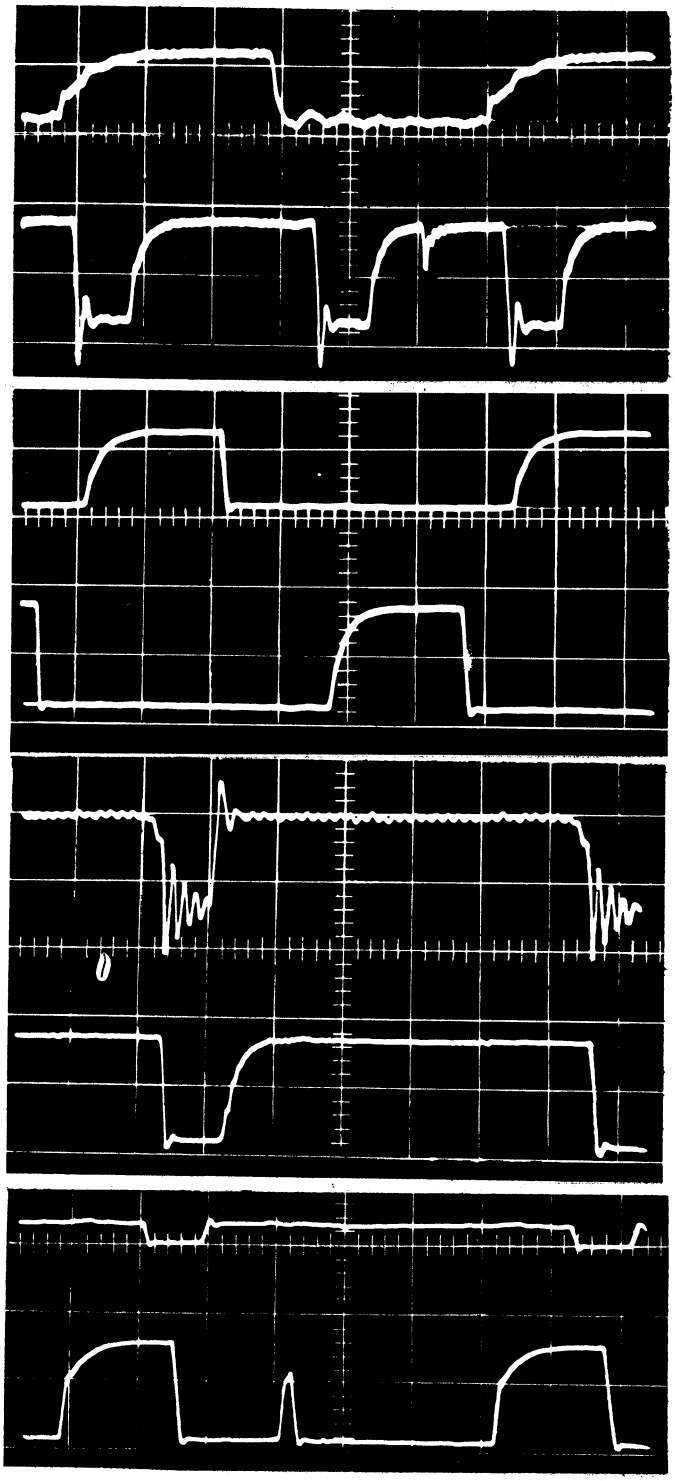


Figure 67. Local Storage Delay Lines (01AD1B2)



+ Read/Write Control
D1B2G09

(Attenuator x 10)

-Local Store Call
D1B2D09

+ Read Gate
D1B2B13

Scope Settings

Sync Point: + Read/Write Control D1B2G09
Sync Mode: External +
Time Base: 0.2 micro seconds
Vertical Amp: 0.2V

+ Write Gate
D1B2D02

Recordings obtained using
Fairchild Type 766H 'scope.

Strobe + 4V to GND
D1B6D05

- Data Out
D1B6B02

- Strobe Driver
D1B2B12

(Minus during Write Gate
time if writing) D1D7

+ Data In

Figure 67.1 Local Storage Control Lines

Diode Changing

If diode or drive line trouble is suspected in local storage, follow LSAR address lines in local store logics through read/write drivers and eventually to the pin numbers on the array cards. (Lines start on ALD LS011.) Once the X and Y drivers have been traced to where they entered the card, land patterns can then be followed to find diodes. Logics show the layout of the array card and diodes. The diodes are of two types: A and B.

To locate a specific array line, read/write lines must also be followed through to where they entered the card. The land patterns can then be traced to the diodes concerned, and from there to the array lines.

Removal of Diodes

1. Remove the suspected faulty card from the logic board.
2. Carefully place the card on a flat work area.
3. Meter the pins of the suspected diodes for a short circuit one way, and equivalent open circuit the other way.
4. If a faulty diode cannot be found, meter the line to check for an open drive line circuit. If a core fault is determined, the card must be replaced; core faults are not considered field-repairable. If a faulty diode is found, proceed to step 5.
5. Unsolder the three diode pin connections, taking care not to apply excessive heat or damage the land patterns.
6. Remove the defective diode and replace it with a tested spare.
7. Inspect the card for damage.
8. Replace the card.

Storage Protect

This procedure tests that the storage protect circuits operate correctly when the voltage is biased ±6 percent.

Marginal Check

1. Load external diagnostic 43C8. This diagnostic cycles the storage under worst case pattern conditions. The diagnostic monitor halt on the error sense switch must be off, so that, after executing the error routine, the diagnostic continues to cycle.
2. With the diagnostic cycling, adjust SP/Vxy ±0.5v (potentiometer on the internal CE panel) from normal (original setting) and note the value of SP/Vxy. The diagnostic should run for one minute on each marginal setting without errors.

If the test fails to run, then the storage voltage operating point should be checked using the following procedure. If the test still fails after operating point voltage adjustment, check for a cause.

Operating Point Voltage Adjustment

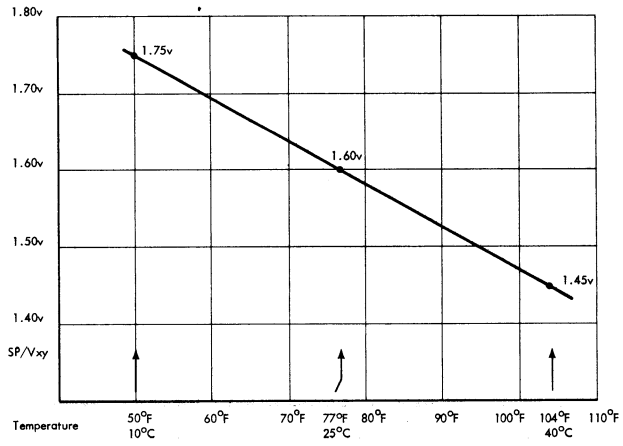
After setting the logic voltages, +6v, +3v, and −3v, to their nominal values, initial adjustments on two potentiometers are required (ALD LV071).

These adjustments, as shown below, are necessary partially to optimize memory performance.

The SP/Vxy potentiometer is on the internal CE panel. The SP/Vsl (sense lever) potentiometer is on the SLT card at 01A-D1J4.

Voltage levels should be checked with a high impedance voltmeter (Branch Office tool, Part 461079).

1. Load and run external diagnostic 43C8 while doing adjustments; 43C8 tests the storage under worst case conditions.
2. At 77 degrees F (25 degrees C) set SP/Vxy to +1.60 ±2 percent. For any other temperature, set SP/Vxy according to the temperature tracking diagram (Figure 68). (The storage protect temperature is 7 degrees F (4 degrees C) higher than the room temperature.) Measure the voltage between pin 01A-D1J4D11 and logic ground (any D08 pin).
3. Connect a meter between pin 01A-D1J4B02 and logic ground (any D08 pin), to indicate the sense level voltage (SP/Vsl).
4. With the diagnostic cycling, decrease SP/Vsl until the first error occurs and note the value (lower limit).



NOTE:
SP/Vxy is defined as the voltage difference between V reference (pin 01AD1J4D11) and logic ground. Because the meter is referenced to -3v, the meter indicates three volts higher than the actual voltage.

Figure 68. Voltage vs Temperature Tracking (Storage Protect)

5. With the diagnostic cycling, increase SP/Vsl until the first error occurs and note the value (upper limit).

6. Set SP/Vsl to a value halfway between the upper and lower limits.

7. After performing the above adjustments, perform the steps in the "Marginal Check."

Array Changing

If any storage protect core plane becomes defective, then one SLT card (4-72) must be changed.

Storage protect is mounted on one card located at 01A-D1K2 (PA821). For storage protect core plane faults, remove the card and repair or replace it.

Diode Changing

To find a faulty diode, trace the address lines on ALD PL701 through storage protect local storage. Refer to "Diode Changing" under "Local Storage" for a complete procedure for finding the faulty diode.

Main Storage

The +60v MS/Vxy and +60v MS/Vz power supplies are temperature-compensated to allow for temperature changes in the arrays. The operating limit of each main storage unit varies inversely with the temperature; as the temperature increases, output from the +60v supplies decrease approximately 0.2v per degree F (0.11v per degree C). When the operating point voltage is established at a given temperature, main storage should operate correctly at all temperatures between 60-90 degrees F (15.5-32.2 degrees C).

Marginal Check

This check procedure tests for sufficient voltage margins around the storage operating point.

1. Run the main storage pattern test for one minute with MS/Vxy and MS/Vz (potentiometers on the internal CE panel) at nominal (present setting) and note the voltage setting of MS/Vxy and MS/Vz.

2. Adjust MS/Vxy voltage a minimum of ±4.5 percent from nominal. The pattern test must run for two minutes without errors on each margin.

3. Press system reset to stop.

If this test fails to run, the main storage voltage operating point should be checked by using the procedure which follows. If checking gives errors after operating point voltage adjustment, check for a cause.

Operating Point Voltage Adjustment ("Shmoo" Graph)

The operating point voltage adjustment may be used as a trouble analysis technique. The bit or bits that are the limiting factors indicate the need for card replacement or strobe adjustment.

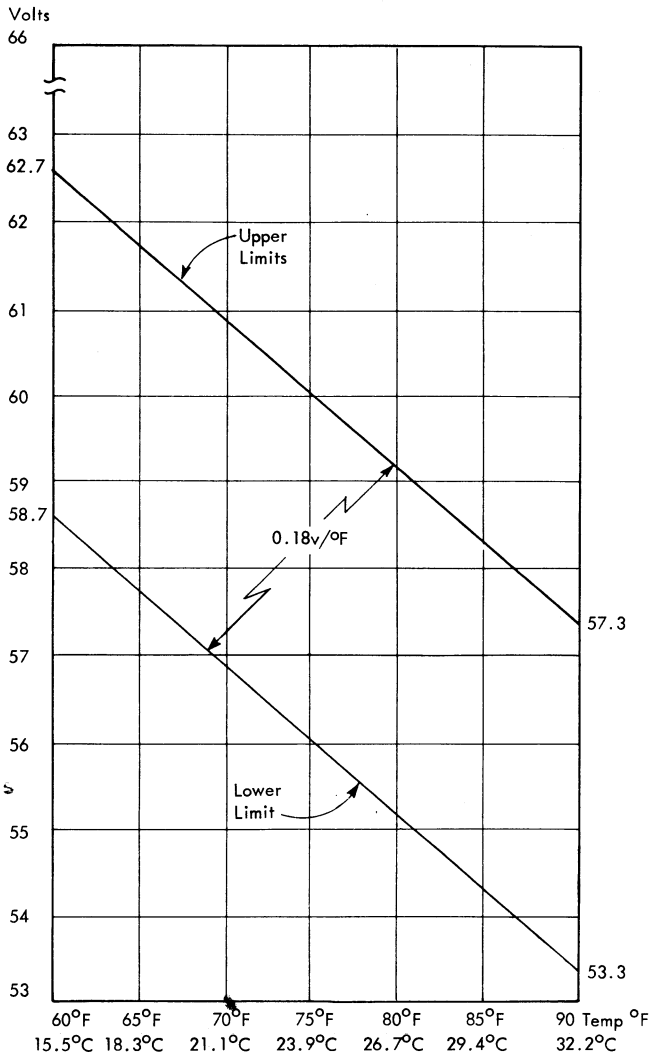
Set the logic voltages, +6v, +3v, and −3v to their nominal levels. These adjustments, as shown below, are necessary to optimize main storage performance. Record values in the following adjustments on a graph such as on ALD MA003.

1. Run main storage internal pattern test with CPU check set to stop and DSAB intvl timer key down.

2. Consider the main storage array temperature to be 3 degrees F (1.7 degrees C) higher than the room temperature. Record this value to be used later.

3. Set MS/Vz to 4 volts less than the lower limit for the recorded temperature, as shown on the MS/Vz tracking chart (Figure 71).

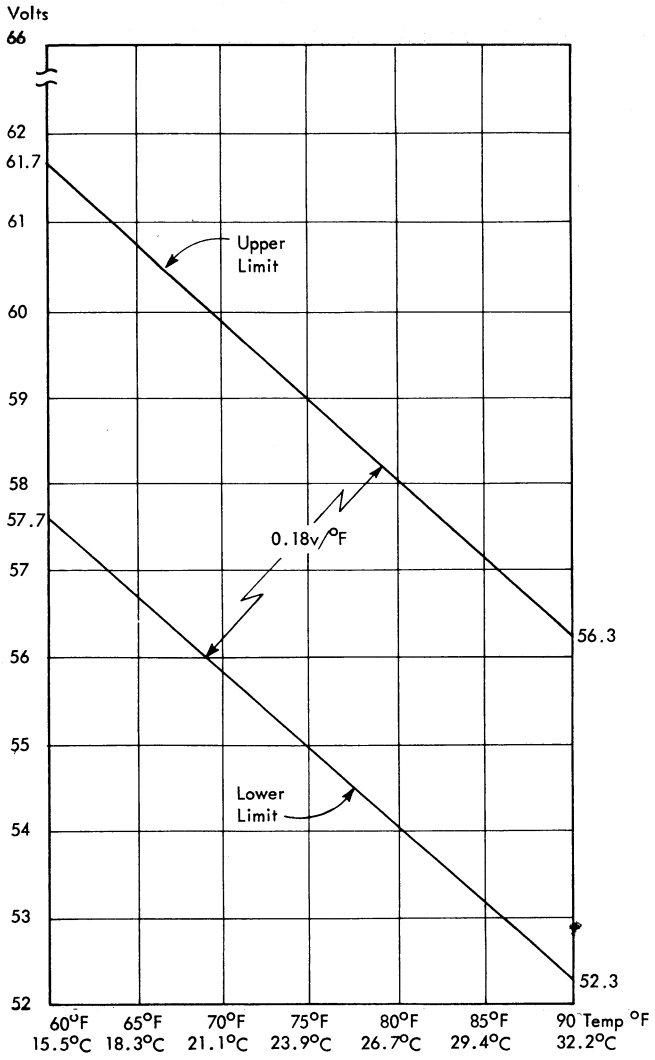
4. Decrease MS/Vxy until the first error occurs and



128K, 64K Byte
X-Y Voltage
Shmoo Point

Note: At a specified temperature, the X-Y center point must fall within the limits shown.

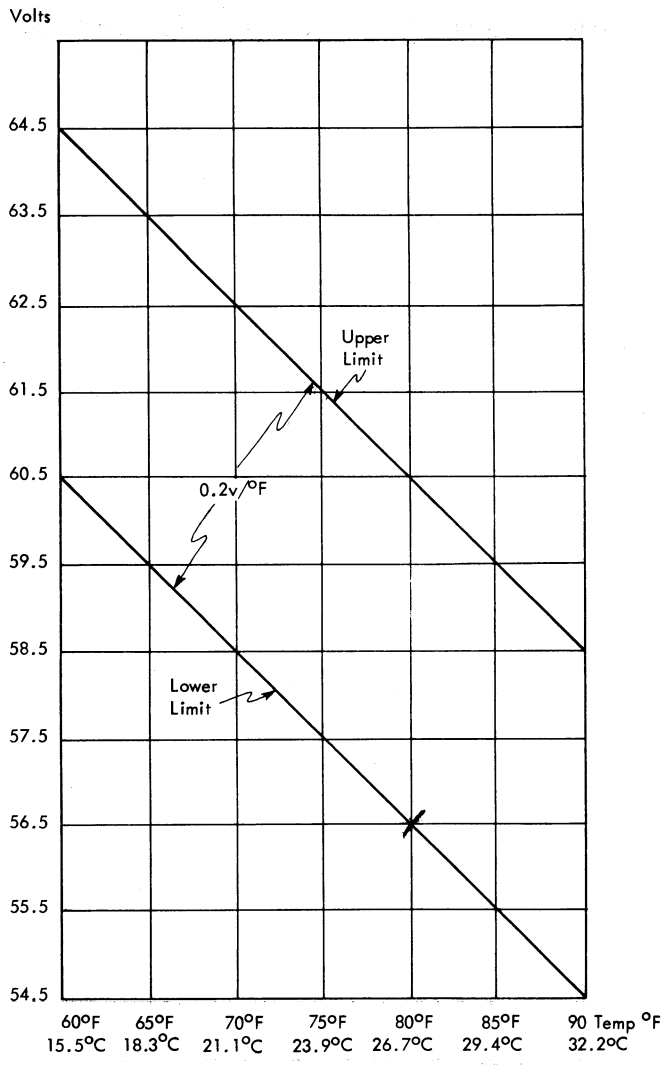
Figure 69. Main Storage Vxy Versus T (128K, 64K)



32K Byte
X-Y Voltage
Shmoo Point

Note: At a specified temperature, the X-Y center point must fall within the limits shown.

Figure 70. Main Storage Vxy Versus T (32K)



128K, 64K, 32K Byte
Z Voltage
Shmoo Point

Note: At a specified temperature, the Z center point must fall within the limits shown.

Figure 71. Main Storage Vz Versus T (128K, 64K, 32K)

then slowly increase MS/Vxy until the pattern test runs without error. Record this value as the lower limit of MS/Vxy. (Note the bit or bits that fail first.)

5. Increase MS/Vxy until the first error occurs and then slowly decrease MS/Vxy until the pattern test runs without error. Record this value as the upper limit of MS/Vxy. (Note the bit or bits that fail first.)

6. Increase MS/Vz in increments of 2v and repeat steps 4 and 5 until MS/Vz reaches a value 4 volts above the upper limit for the previously recorded temperature (Figure 71).

7. When steps 4, 5 and 6 have been completed, connect the upper limiting points together; connect the lower limiting points together. Inscribe within these limits the largest possible circle tangent to the upper and lower operating points. The center of this circle will be the operating point voltage of MS/Vxy and MS/Vz.

8. The limits of MS/Vxy and MS/Vz from the above operating point voltage must be equal to or greater than ±4.5 percent. The operating point voltage must also fall within the tolerances given for the temperature recorded in step 2 (see Figures 69, 70, and 71 for tolerances). If this minimum percentage cannot be met, review the limiting bits to determine if any one bit is consistent; this may indicate the need for card replacement and/or strobe adjustment.

9. After making any strobe adjustments or replacing

a card to improve the limits of MS/Vxy, repeat steps 4, 5, 6, and 7.

10. Check Mpx storage at the nominal operating point voltages.

11. Record the MS/Vxy and MS/Vz operating point voltage value and the temperature on ALD MA003.

M-7 storage timing is shown in Figure 72 and 72.1.

Strobe Checking

Main storage strobe should be adjusted only when:

1. A main storage voltage adjustment procedure shows that the operating point is no longer within tolerance.
2. Repetitive failure of bit positions or sense amplifier cards occurs.
3. A main storage error cannot be cleared by any other means.

To check:

1. Set up the main storage worst case pattern test to run in enable mode. CPU check to stop; DSAB INTVL TIMER key down. Refer to "Delay Line Tap Changing" to check the delay line board pin numbers.
2. Unwrap the 5-nanosecond strobe connection (Figure 76), then use a wire shorting link to facilitate these checks. The location of the byte in the array determines which strobe will be used. They are divided as follows:

ADDR BIT	STROBE A	STROBE B
	Byte 0 Bits 9-17	Byte 1 Bits 0-8
	Byte 1 Bits 0-8	Byte 0 Bits 9-17

3. With MS/Vz at the previously established operating point, advance the strobes in 5-nanosecond increments. Adjust MS/Vxy to find the error-free upper and lower limits. Subtract the lower limit MS/Vxy voltage from the upper limit MS/Vxy voltage and record the difference along with the delay line tap setting of each strobe. Continue until the difference starts to decrease.
4. Repeat step 3, retarding the strobes in 5-nanosecond increments from the original operating point.
5. Set the strobe at the point which gave the greatest difference. Perform "Operating Point Voltage Adjustment."
6. The new operating point voltage should conform to the specifications called out in the operating point voltage adjustment procedure. If it does not, determine the limiting bits and addresses, and review the graph previously plotted. Possible causes of error are: sense amplifier card, final amplifier card, gate card, or improper strobe adjustment.
7. Record "shmoo" graph points of MS/Vxy and MS/Vz, temperature, and strobe settings for future reference (ALD MA003).
8. Run all main storage external diagnostics before returning the system to the customer.

Delay Line Tap Changing

Nine sets of delay lines are used in main storage logic. Six sets of delay lines have 25-nanosecond taps and three have 5-nanosecond taps. Three 25-nanosecond tap delay lines are mounted on two SLT cards and are located at 03A1 C6 and 01A1 F6. The 5-nanosecond tap delay lines are located on the SLT card at 03A1 B6.

Main storage logic is timed from these delay lines, but normally you need to adjust only the timing of the strobe pulses. The strobe pulses are adjusted by wire wrapping on the pin side of main storage logic board 03A1 and are taken from a combination of two 25-nanosecond tap delay lines and one 5-nanosecond tap delay line. The combination is adjusted either to advance or to retard the strobe timing.

Figure 76 shows strobe A wired to be active after a 490-nanosecond delay; strobe B is wired to be active after a 485-nanosecond delay. Figure 77 shows the back panel wiring.

Service Hints

Singleshots

During the first part of a read cycle, the 450ns singleshot on ALD MA031 prevents any read reset pulse. If the singleshot does not fire when impulsed, check the 18-volt power supply.

Scoping Main Storage

Write control at A1H6J07 is a good sync for scoping main storage (especially clock circuits).

Read/Write Driver Timing

X read/write driver timing at A1H6B07 and Y read/write driver timing at A1H6J05 should be a 2.5- to 3.0-volt pulse. If the pulse is less than 2.5 volts, driver current decreases and causes random failures. If main storage cannot read zeros, check that strobes A and B are present at A1J6J04 and A1J6G12 respectively.

Delay Lines

Figure 71.1, A shows the positive pulse on the input and output of the delay line driver. If the output of the delay line driver looks like that in Figure 71.1, A but ghost pulses appear between the normal pulses, the delay is open and the card should be changed. If no pulse is on the output, replace the line driver. If changing the card does not yield a pulse, the delay line

is probably shorted. Check the yellow timing wires associated with the delay line card to see whether any wires are pulled so tightly around a pin as to cause a short.

Drive Lines

Use a current probe to check drive current on the gray wires going to card B1M2 (X current – pins G03 and J04, Y current – pins D12 and B12). Figure 71.2 shows a simplified drive circuit.

Good X Current is shown in Figure 71.1, B. The read pulse is longer in duration than the write pulse.

Good Y Current is shown in Figure 71.1, C. The read and write pulses are of about the same duration. A read cycle has a larger stagger between terminator gate turn-on and drive current turn-on.

Drive Lines Shorted Together: Figure 71.1, D is a current indication of two drive lines shorted together. The pictures in Figures 71.1, D and 71.1, E were taken while cycling one-quarter of main storage. If all of main storage is cycled, the trace is very light.

To locate a defective drive line physically (shorted or open), loop on the failing address and lightly run a voltage probe down the drive lines on the array. A +60 volt level indicates an unselected drive line; a voltage drop indicates the selected drive line. Figure 71.1, F shows a short; Figure 71.1, G shows an open drive line.

The indication in Figure 71.1, F appears on the shorted line and on the line (probably an adjacent line) to which it is shorted. Once the shorted lines are isolated, step an ohmmeter across the array on the shorted lines until the least resistance is measured (resistance = approximately zero). Examine the area for the cause of the short. Possible causes are: drive line pins touching or a metal chip between the pins (the chip may be wedged under the rubber seal between planes).

If the shorted lines are not adjacent lines, try replacing the gate cards (4196) associated with the shorted lines (ALD MD030).

Drive Line Shorted to Ground: Some possible causes of a grounded drive line (Figure 71.1, H) are:

1. Inhibit resistor assembly – If the X current is failing, check the inhibit resistor assembly on the B side of the array (Figure 73) to make sure the assembly is not shorting to the X drive lines.

2. Stand off – One of the yellow and black wires that go to the pins on the array are pinched between the stand-offs. Three stand-offs are on the B and D sides of the array; one stand-off is on the A and C side between the D1 board and the front frame casting.

3. Shorted limiter – To isolate the gate card with the shorted limiter, watch the defective current, and pull gate cards one at a time. When the defective gate card is pulled, the waveform looks like the open drive line in Figure 71.1, G.

4. Driver card (4904) – One of the orange drive lines from the driver card on the B1 board to the array interface or a transistor in the driver card (4904) is shorted.

5. Defective gate clamp card (3588).

Open Drive Line: To locate an open in the suspected drive line (Fig. 71.1, G), step a voltage probe across the array on the open line. When the probe goes past the open, the waveform changes polarity (inverts). When the area of the open is located, check the drive line welds for secure bonding. The weld may be on either side of the array because the drive line zigzags across the array. If the weld is good, use an ohmmeter to isolate the open.

Driver Current Turn-Off: Driver current turn-off should occur before terminator gate turn-off. If the current is being turned off by the terminator gate turn off, unwanted noise in the array and bit failure may occur (Figure 71.1, I). To correct this trouble, replace the gate cards (4196) or drivers (4904) that have late turn-offs. A read current amplitude that is twice the write current amplitude, or vice versa, indicates a bad gate terminator card (4889).

Sense/Inhibit Lines

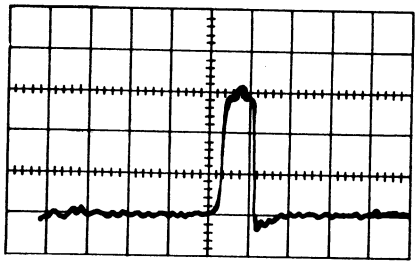
Sense circuits and inhibit circuits use the same blue and white wires from logic boards A1 and B1 to the array. The resistance of each leg of a sense/inhibit line to ground should be 7.5 ohms. The resistance between the blue and white wires at the output of the sense/inhibit card (4927) should be 15.0 ohms. A normal inhibit pulse at the output of the sense/inhibit card, on either the blue or the white wire, is shown in Figure 71.1, J.

Open Sense/Inhibit Line: The waveform resulting from an open in either leg of the sense/inhibit line is shown in Figure 71.1, K. When an open in the sense/inhibit line is detected, check the following items:

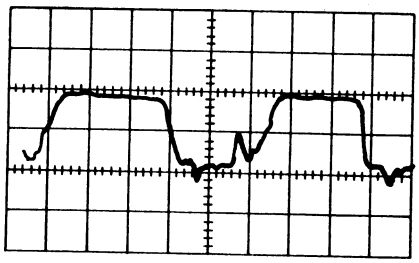
1. Continuity of the blue or white wire from the sense/inhibit card (4927) on the A1 or B1 board to the wire welds on the B side of the array.

2. The welds of the small jumpers (chairs) on the D side for the plane or segment that is in error.

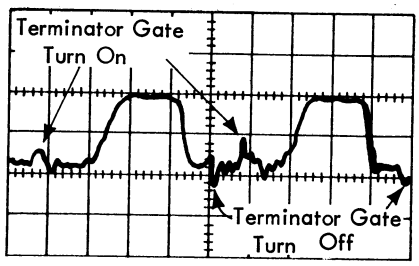
3. The welds on the inhibit bus on the B side of the array.



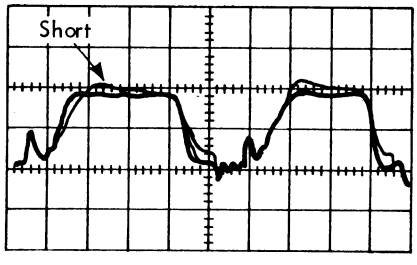
A. Input to Delay Line Driver



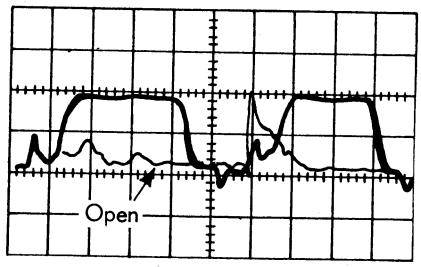
B. X Drive Current (380 - 400 ma)



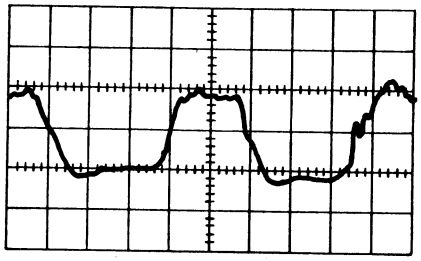
C. Y Drive Current



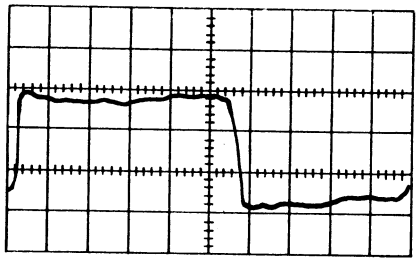
D. Shorted X Drive Line



E. Open Drive Line (Current Measurement)



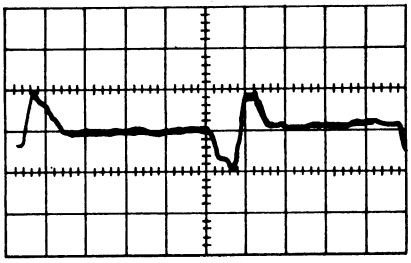
F. Shorted Drive Line



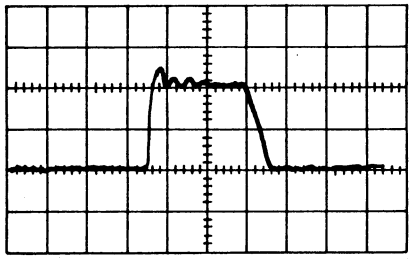
G. Open Drive Line

Figure 71.1. Main Storage Scope Traces (Sheet 1 of 2)

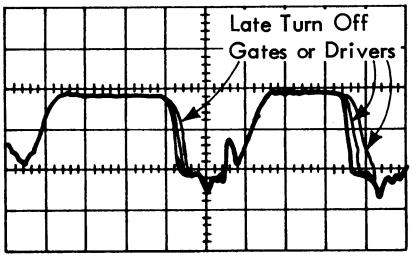
Done with current probe



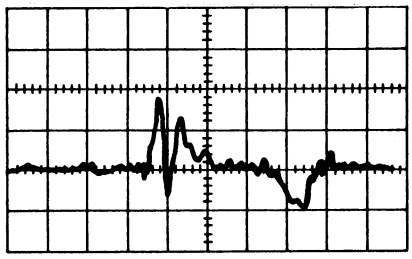
H. Drive Line Shorted to Ground



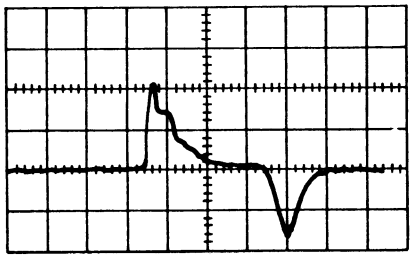
K. Inhibit Pulse with Open Sense/ Inhibit Line



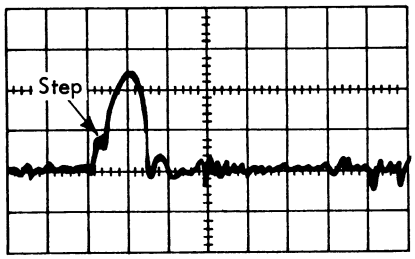
I. Late Gate or Driver Turn Off



L. Inhibit Pulse with Grounded Sense/ Inhibit Line or Shorted Inhibit Driver



J. Good Inhibit Pulse



M. Good Sense Amplifier Output

Figure 71.1 Main Storage Scope Traces (Sheet 2 of 2)

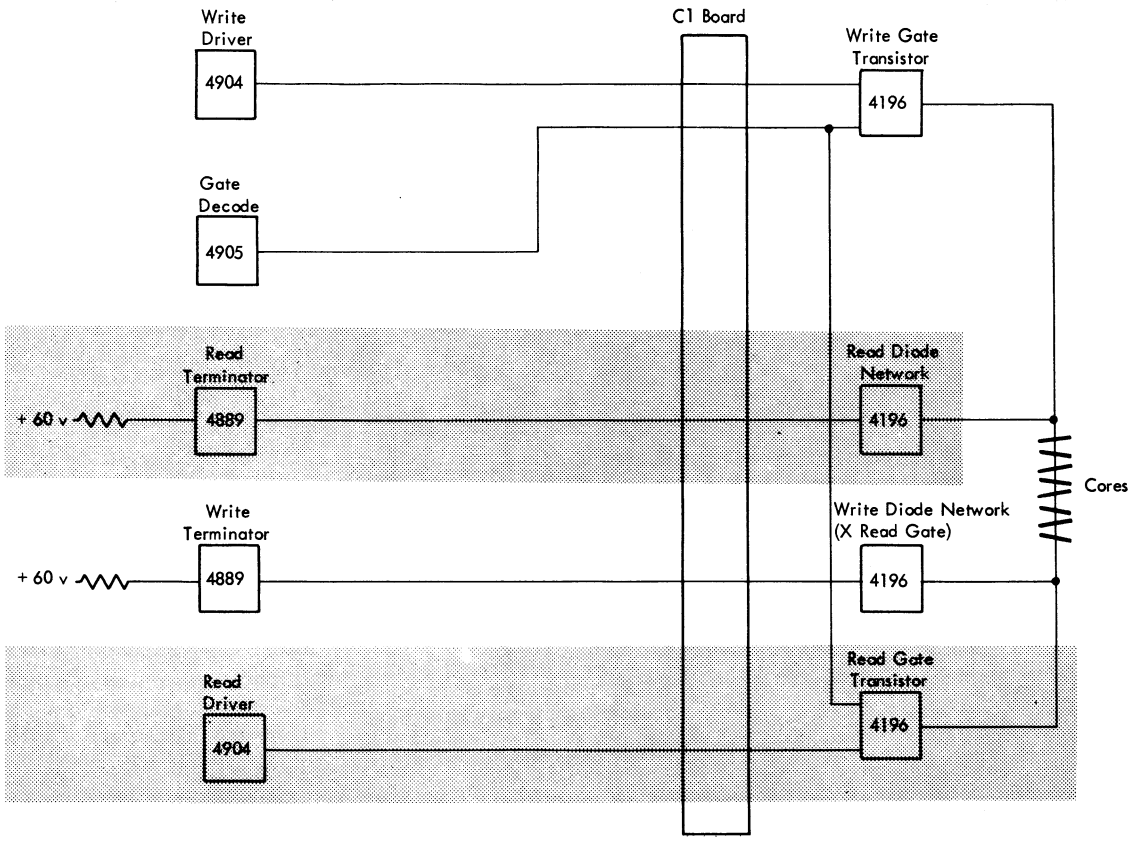


Figure 71.2 Simplified Drive Circuit

Grounded Sense/Inhibit Line: Figure 71.1, L shows the waveform of a grounded sense/inhibit line or a shorted inhibit driver transistor. If three segments are in error and one is not, replace the sense/inhibit card (4927) for the segment that is not in error. If the waveform does not change, check the blue and white wires for a ground. To isolate a ground in the array, pull the paddle card on the C1 board for the suspected bit and segment (ALD page MD020).

Memory Timing

Use Figure 71.3 as a reference when changing memory timings.

Strobes A and B

Figure 71.1, M shows the output of a sense amplifier card (4927). Check that the width of the strobes is 200-275ns.

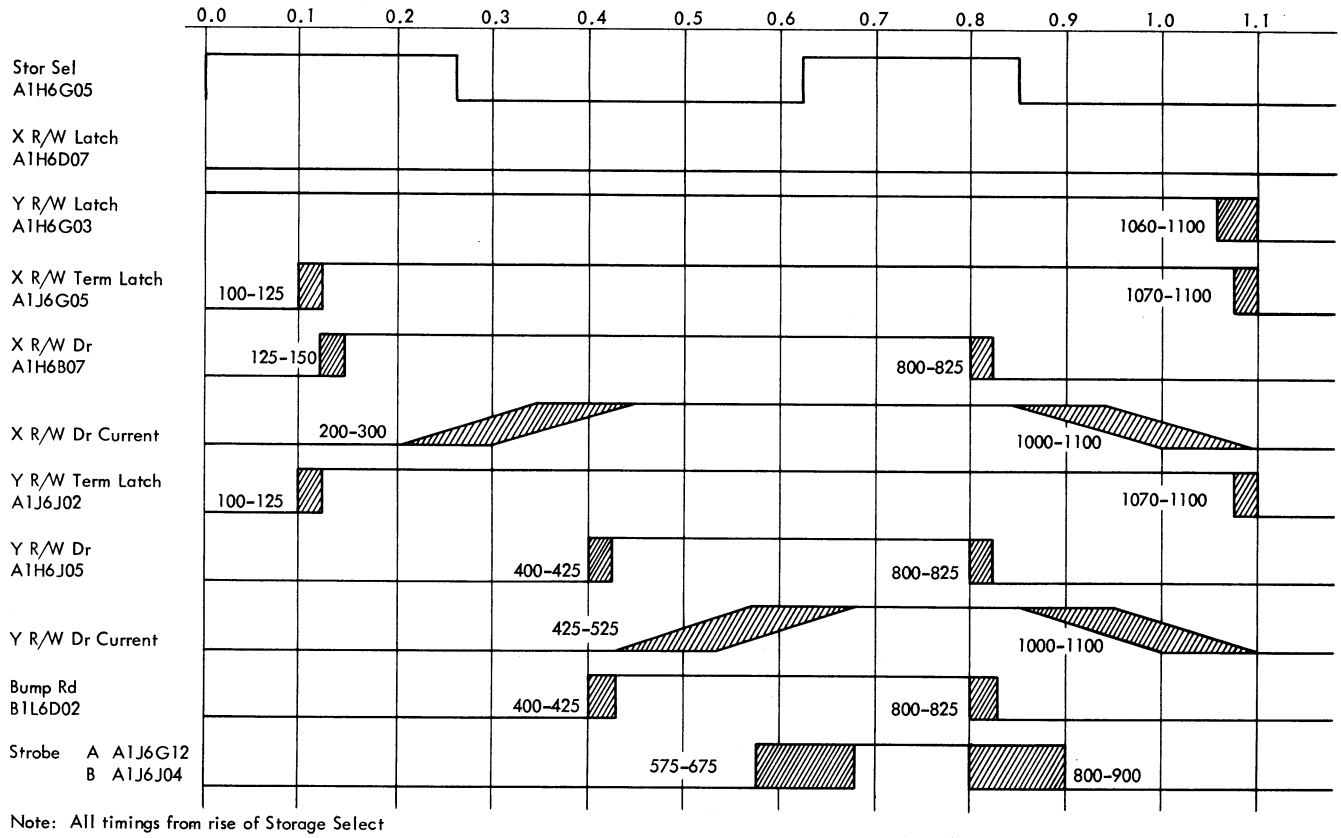
To get the strobes in the approximate area of best operation, look at the sense amplifier output and set the strobes so that a small step (not more than 60ns) is on the leading edge of the pulse. If no step is present, strobe turn-on is too late; if the step is too long, strobe turn-on is too early.

For a final adjustment, run a schmoo and adjust strobe timing for the best possible schmoo.

If a bit drops when the XY voltage is lowered, try setting the strobe (associated with that bit and segment) earlier. If a bit picks when the XY voltage is raised, try setting the strobe (associated with that bit and segment) later.

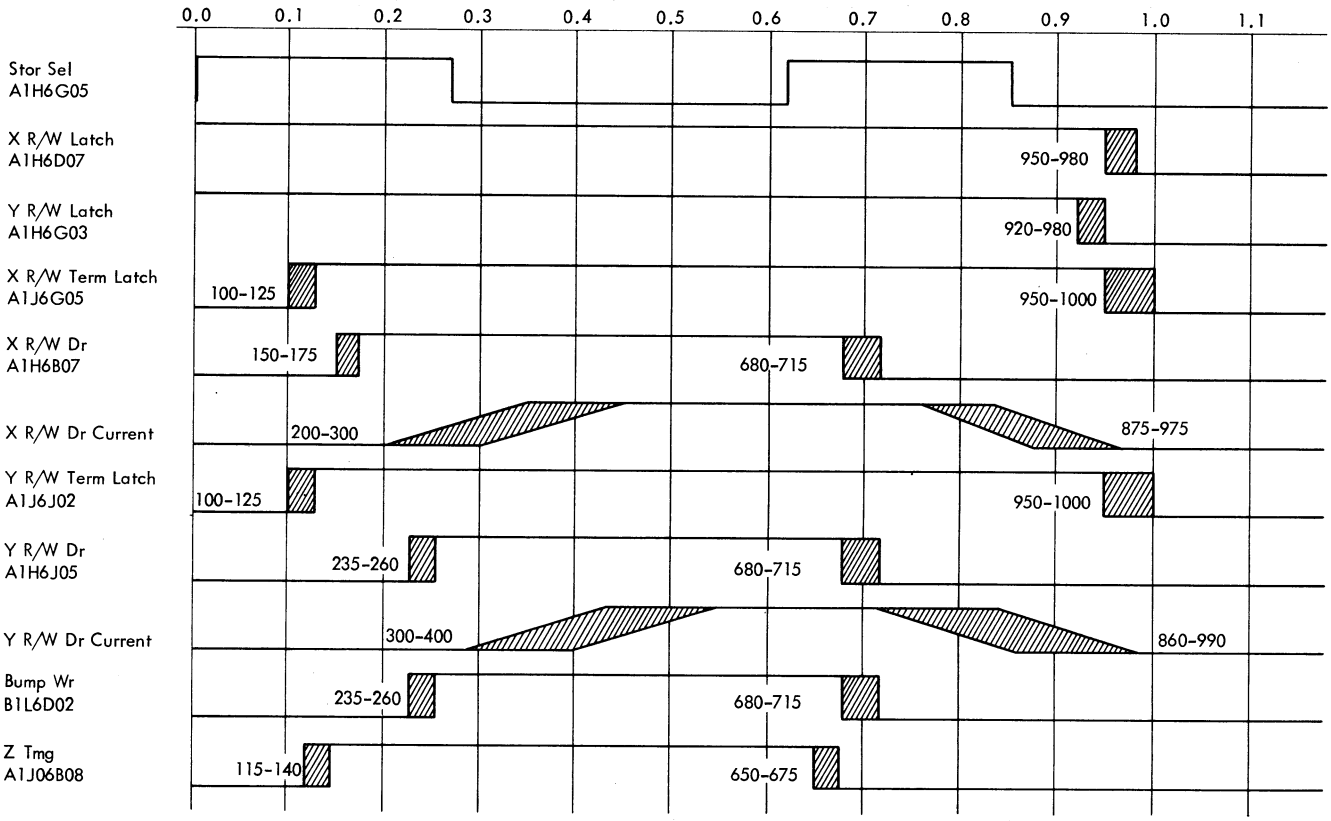
Pulse Function	Scope On	Ref Pt	Comments/Notes	Turn On Min	Turn On Max	Adjust Tap	Turn Off Min	Turn Off Max	Adjust Tap
135ns Singleshot	H6B08		Adjust Lower Potentiometer						
450ns Singleshot	H6D09		Adjust Upper Potentiometer						
Storage Select (T-0)	H6G05		Duration 220-500						
Storage Select (T-1)	H6G05	T0	Duration 220-500	1100	1100				
Write Latch	H6G10	T1					950	980	E6B10
X R/W Latch	H6D07	T1					950	980	E6B13
Y R/W Latch	H6G03	T0	P/R Bit On				1060	1100	D6G07
Y R/W Latch	H6G03	T1	P/R Bit Off				920	950	D6B08
X Read Term Timing	J6G05	T0		80	140	D6D13	1070	1100	E6J10
X Write Term Timing	J6G05	T1		80	140	G6D05	920	950	D6B12
Y Read Term Timing	J6J02	T0		80	140	G6B08	1070	1100	D6G09
Y Write Term Timing	J6J02	T1		80	140	G6B12	920	950	D6D05
Allow Write	J6B04	T0	EC Change	950	1075	F6J05	1600	1760	XXXX
Z Timing	J6B08	T1	Turn on is landed	60	120	E6G07	600	675	E6B12
X Read Current	Current Probe	T0	Time to 50% turn on, 10% turn off	280	330	G6J10	940	990	E6B08
X Write Current	Current Probe	T1	Time to 50% turn on, 10% turn off	315	365	G6J09	780	830	D6B13
Y Read Current	Current Probe	T0	Time to 50% turn on, 10% turn off	570	620	G6G09	940	990	E6D13
Y Write Current	Current Probe	T1	Time to 50% turn on, 10% turn off	415	465	D6J04	780	830	E6D05
Strobe A	J6G12		200 to 275ns						
Strobe B	J6J04		200 to 275ns						

Figure 71.3. Main Storage Timing Chart



Note: All timings from rise of Storage Select

Figure 72. M-7 Storage Read Timings



Note: All timings from rise of Storage Select

Figure 72.1. M-7 Storage Write Timings

Array Changing

If any part of a core plane becomes defective, then the array holding that plane is changed. Each array is 32K halfwords, and Figure 73 shows array positions within the main frame for a 64K storage.

Figure 74 is a guide to the removal of a storage unit holding an array.

Removal Procedure

1. Disconnect the fan and thermal cables from the tag board on the rear of the storage unit fan.
2. Pull out the flat cable connectors from the receptacle.
3. Unscrew locking unit and hinge studs, top and bottom. The storage unit can now be removed and placed on a level surface for further stripping.
4. Unscrew the four holding screws and remove the SLT card cover. The SLT cards can now be removed.
5. Unscrew the fan unit retaining screws. The storage unit has now been partially stripped, leaving only the array and various mounting brackets.
6. Strip the array down to the level of the spare (or replacement) array.

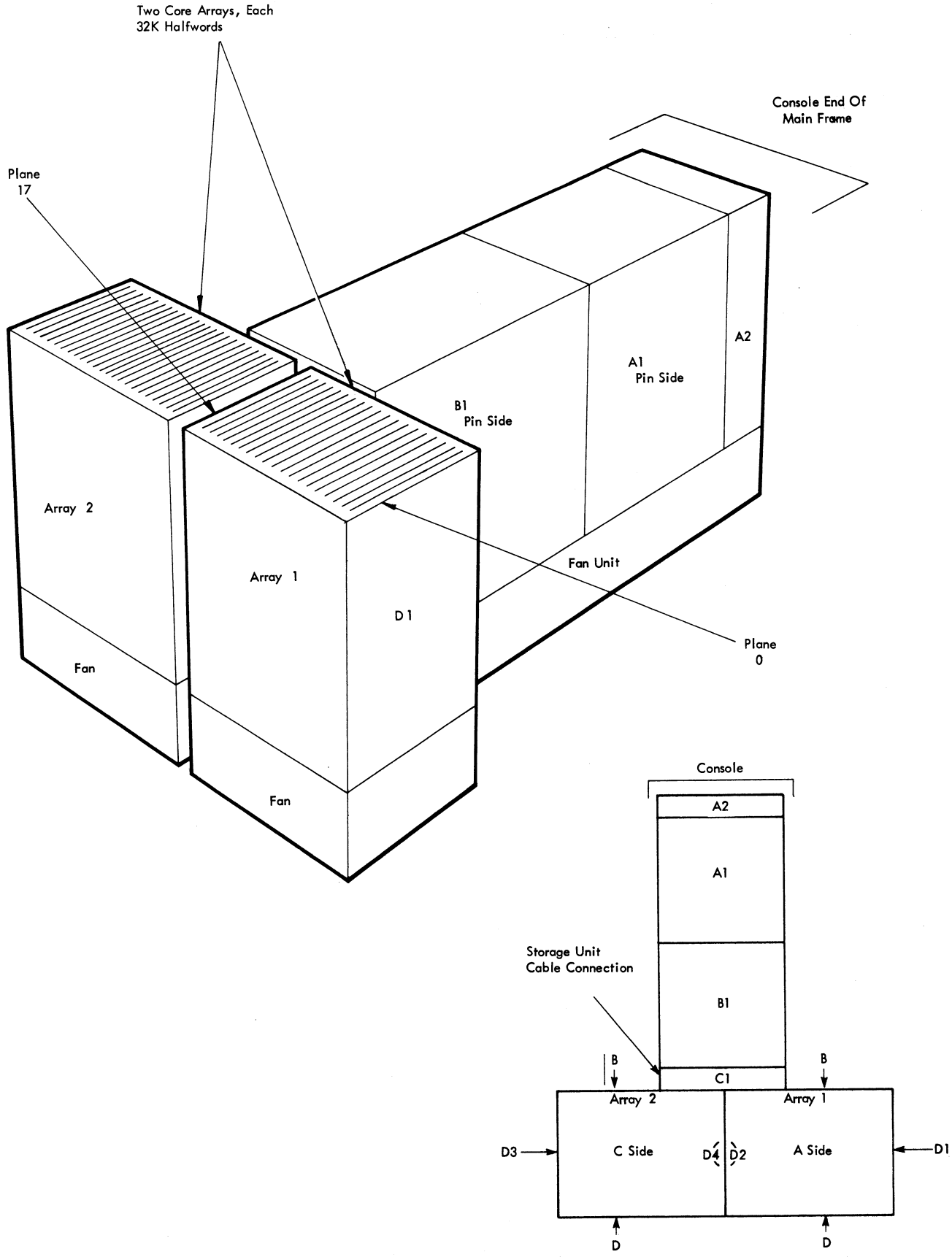


Figure 73. 64K Main Storage (Layout in Main Frame)

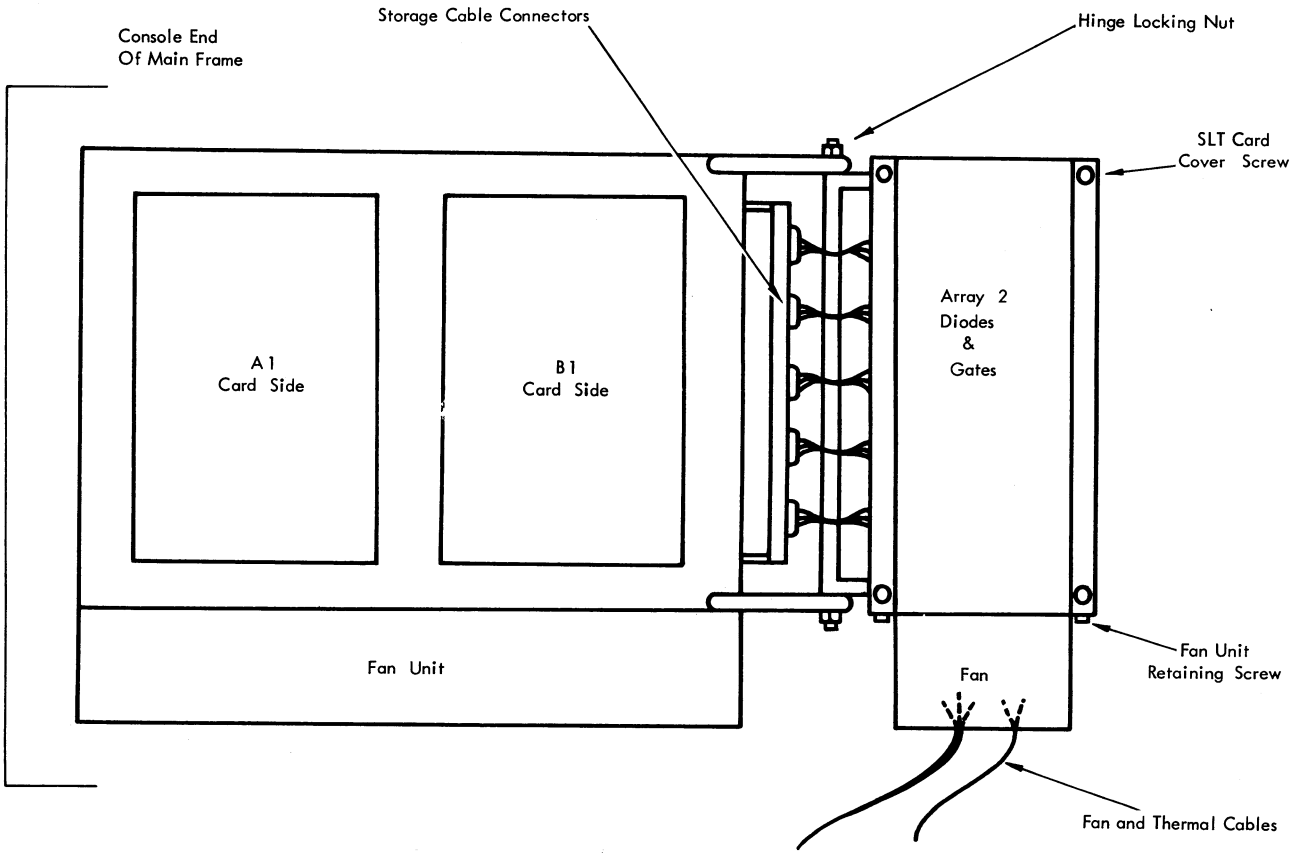


Figure 74. Changing a Storage Unit

Replacement Procedure

1. Reverse the removal procedure and use Figure 75 to connect the cables.

2. After installing the new storage unit, storage voltages must be adjusted to define the best operating point.

3. Use the voltage adjustment procedure detailed in "Main Storage."

If the strobe pulse requires adjustment, use the procedure outlined in "Delay Line Tap Changing."

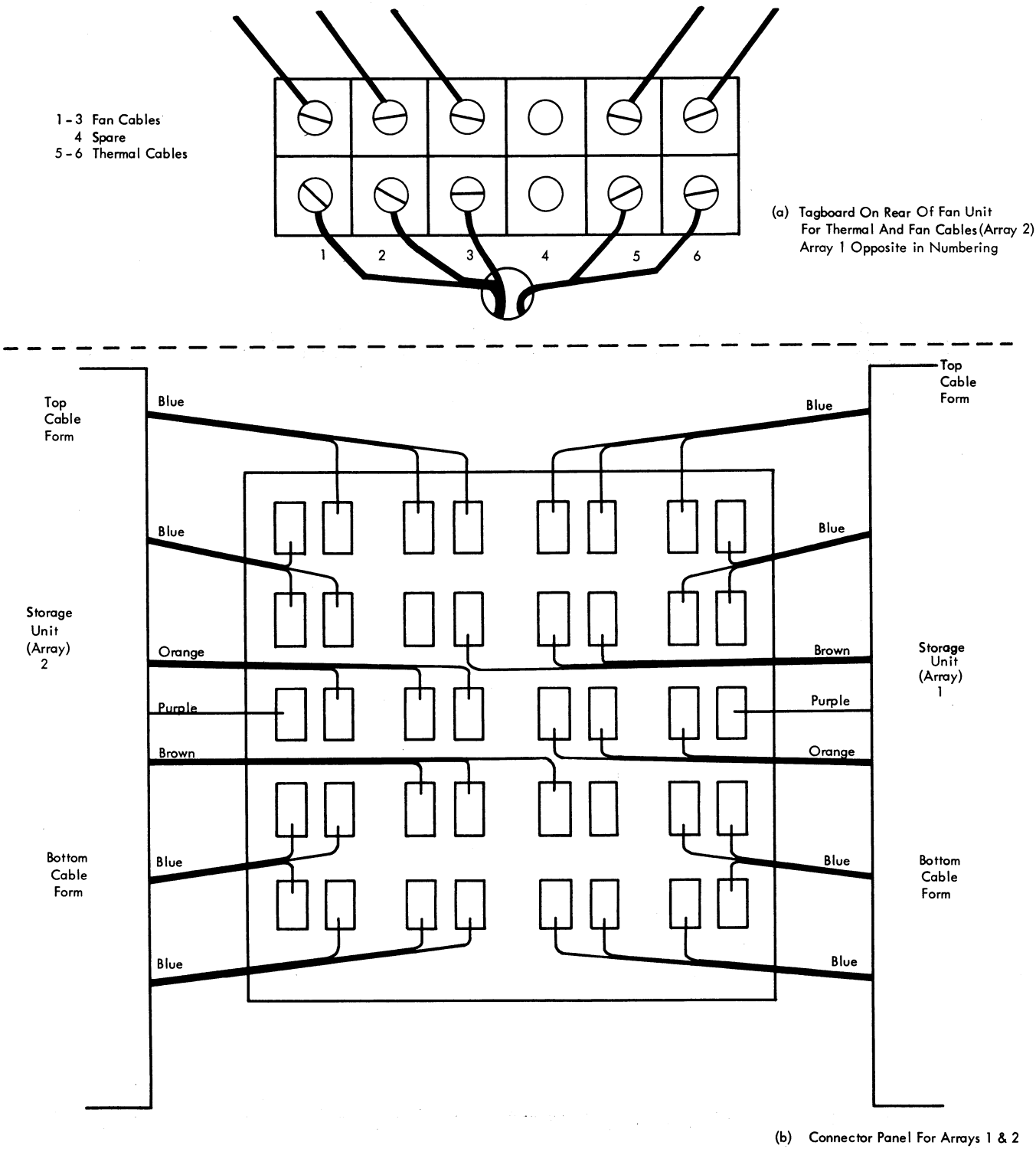


Figure 75. Storage Unit Cable Connection

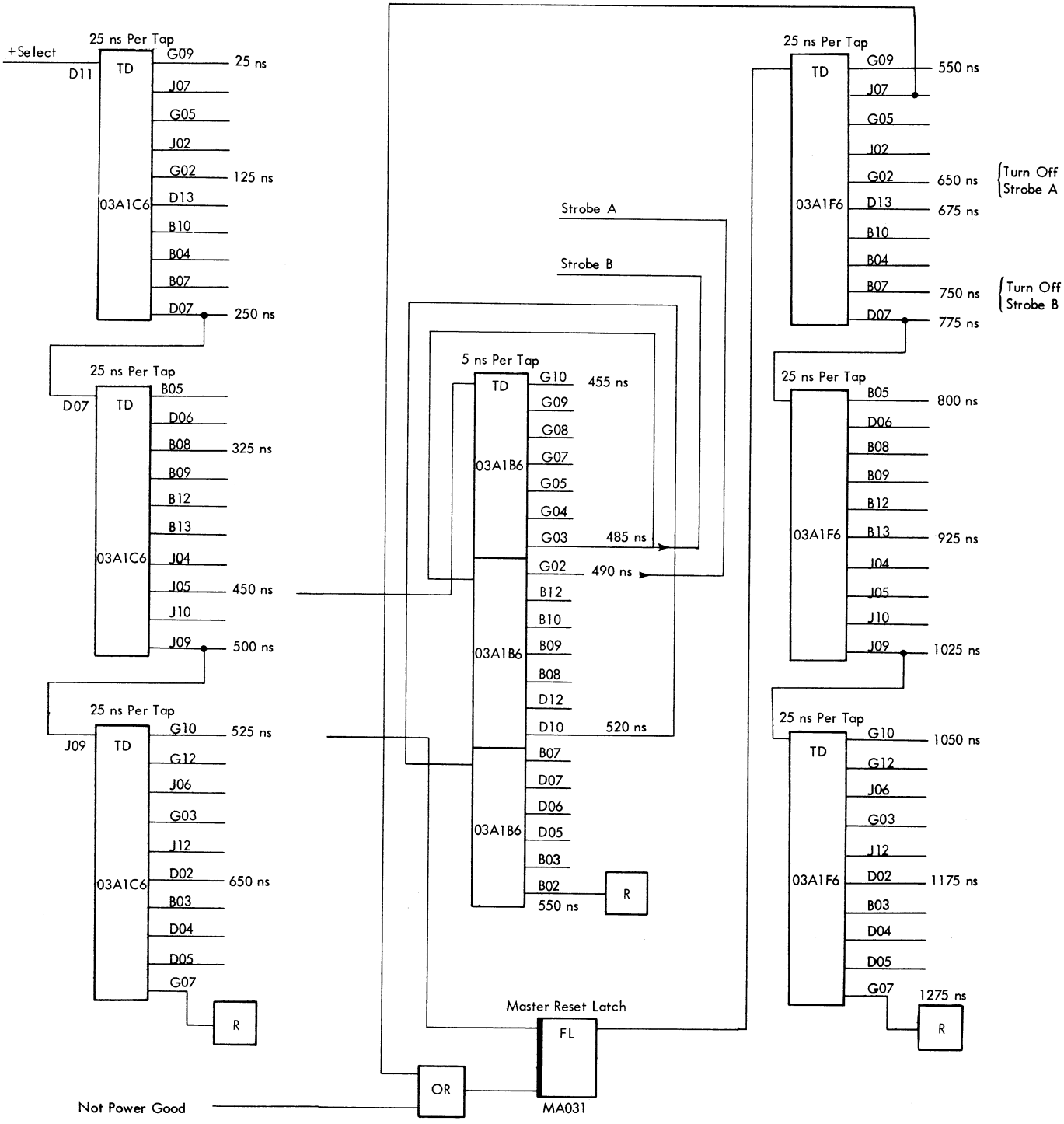


Figure 76. Delay Line Circuits with Locations and Pin Numbers

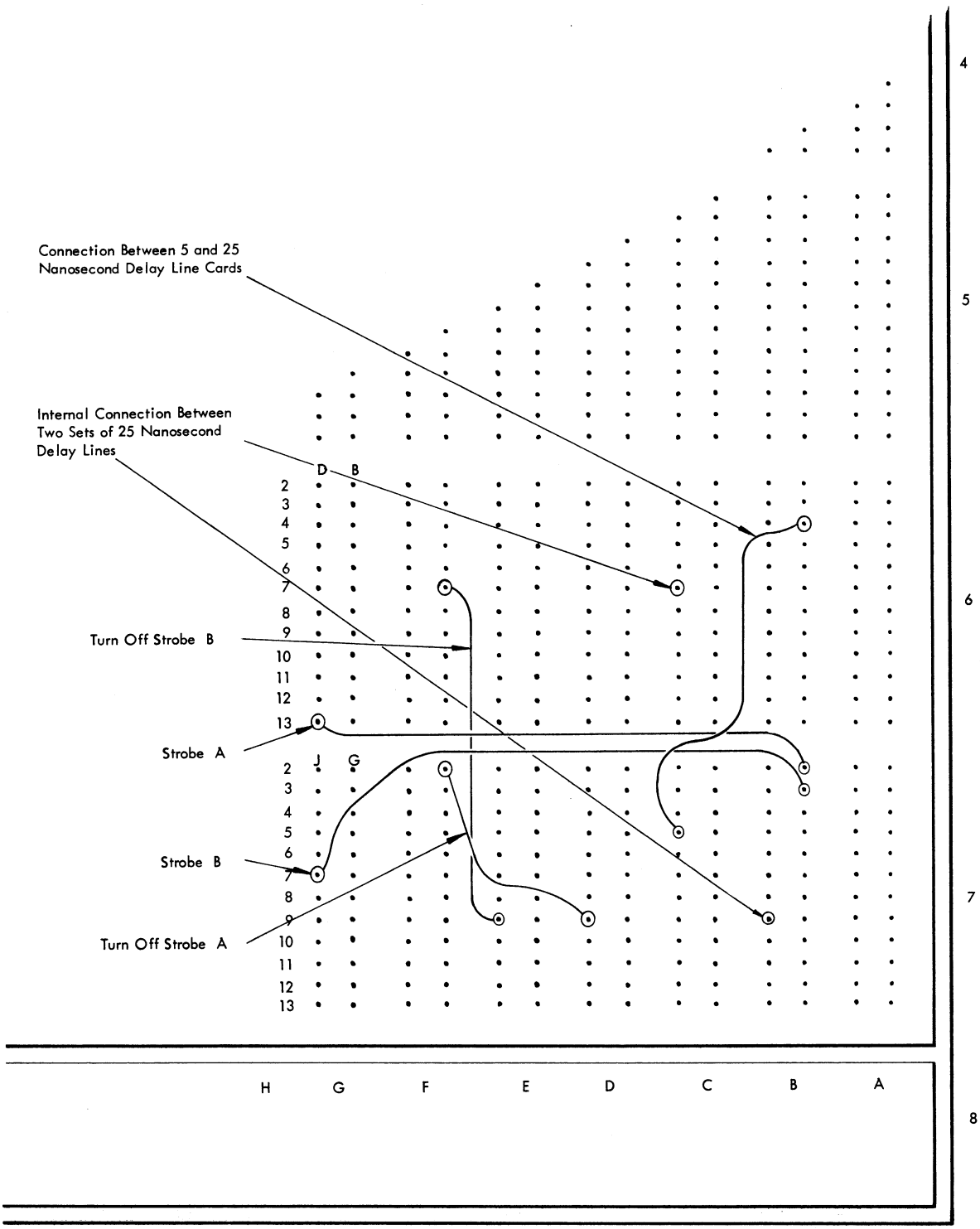


Figure 77. Panel A1 Pin Side (Example of Delay Line Wiring)

Main Frame

Fan Changing

All fan locations are shown in Figure 78. The filters are all located on the input side of the fans. Change the fans as follows:

Main Storage Arrays

1. Swing out the array.
2. Disconnect the power connections from the fan unit.
3. Hold the fan unit and remove the six securing screws. These screws are underneath the unit.
4. Remove the fan unit. Repairs or replacement can now be carried out.

Main Storage Logic

1. Disconnect the fan power cables from the terminal block above the fan unit.
2. Unscrew the six knurled Allen screws that hold the fan unit to the frame. They are located from the top, and there are three on each side of the unit.
3. Move any intruding cable forms away from the 1052 socket side of the fan unit.
4. Slide the fan unit, horizontally, out of the IBM 1052 socket side of the main storage logic frame. Repairs or replacement can now be carried out.

TROS Logic

1. Disconnect the power cables from the card side of the unit.
2. Unscrew the two screws on the same side and slide the unit out horizontally. Repairs or replacement can now be carried out.

Logic Gates

1. Swing open the logic gate.
2. Disconnect the fan power plug on the inside end of the gate fan unit.
3. Release the clip on the outside end of the gate fan unit.
4. Hold the unit, drop downwards, and pull outwards. This unhooks the inside unit holding clip. Repairs or replacement can now be carried out.

Power Supply

1. Remove the four screws retaining the converter inverter cover.
2. Remove the cover. This exposes the converter inverter unit which is modular packed. The fan is mounted vertically and is part of the bottom right-hand module in the converter inverter unit.

To remove the bottom right-hand module:

1. Remove the six-way plug.
2. Disconnect the large diameter cables which stretch between the converter inverter cable loom and the module terminal board.
3. Disconnect any other cables which might foul the module as it is pulled out horizontally, such as those connected to the wave shaping filter terminal board.
4. Remove the module retaining screw. This screw is on the left side of the module about 4 inches up from the bottom of the converter inverter unit.
5. Slide the module out horizontally. Take care not to damage the two fan power cables which are still connected and which, while allowing the module to be removed, prevent the module from being taken away from the converter inverter unit.
6. When these two cables are exposed, cut them at a point about 6 inches away from where they disappeared into the fan motor.
7. Place the module on a level surface.
8. Remove the four screws that hold the fan unit to the module.
9. The fan unit can now be removed from the module for repair or replacement.
10. To replace the fan, attach the fan to the module. Splice the cables that you cut in step 6 and reverse the removal procedure.

Logic

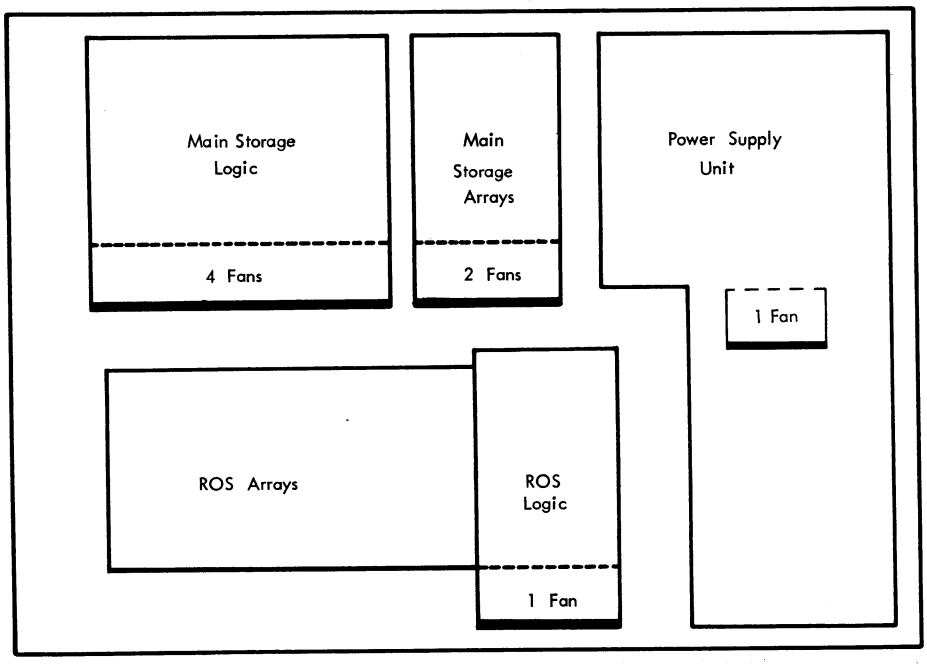
For all logic changes, locate components by using either control panel plugboard section charts or "Locations."

Board Changing

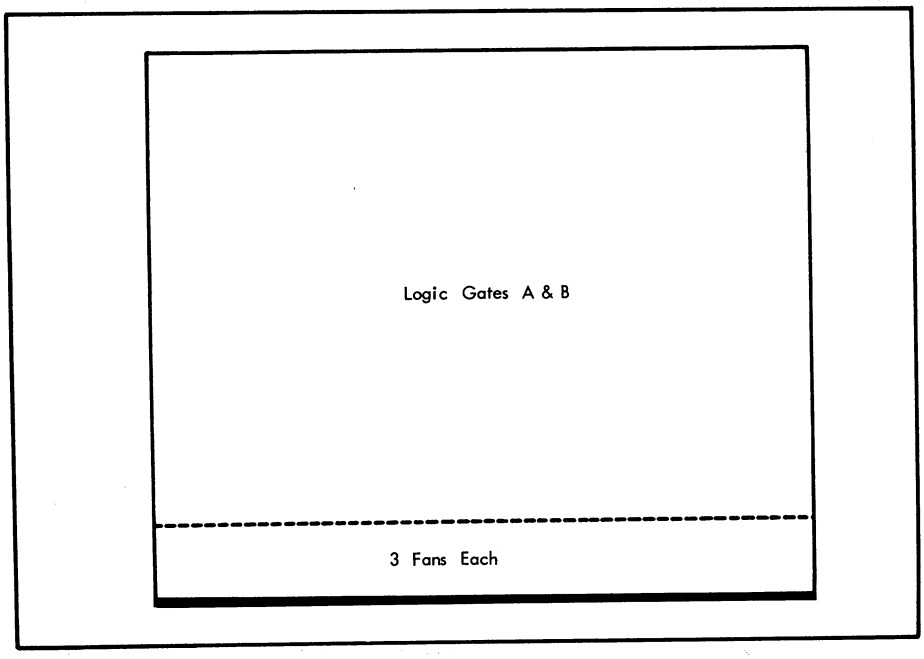
The boards used to hold SLT cards throughout the CPU are held by eight Allen screws and can be removed easily after all components and connections have been removed. Board changing may become necessary if an EC change alters the board land pattern or if a board becomes damaged.

Change the board as follows:

1. Expose the component side of the board.
2. Remove the SLT cards, noting their locations (card plugging chart is available in ALD's at ZC501).
3. Remove the external flat cable connectors and fold them back into the routing slot which corresponds to their locations.
4. Remove the board-to-board flat cable connectors and fold them into the gap between the two frame members.
5. Expose the board pin side and remove any external connections. Note their locations, then fold them back out of the board area.
6. Unwrap carefully any external wire wrapped



CPU MAIN FRAME - MEMORY SIDE



CPU MAIN FRAME - LOGIC GATE SIDE

Note: Dark areas represent filters to be changed according to preventive maintenance schedule.

Figure 78. Allocation of Fans and Filters

connections, using the special CE tool provided, P/N 452527. Note their locations and fold them out of the way.

7. Remove the eight Allen screws and remove the board. Replacement procedure is the reverse of the removal procedure. If the board land pattern has changed, some external connectors may have new locations. This should be clearly noted in the instructions accompanying the new board.

Board Pin Changing

Follow the instructions in the *Solid Logic Technology Packaging, Tools, and Wiring Change Procedure, Field Engineering Manual of Instruction,* Form 223-2800.

SLT Card Changing (Card Puller P/N 452542)

For SLT card changes, simply pull out or plug in. When changing cards, care must be taken to keep them perpendicular to the board surface. Also, certain cards, such as main storage logic and local storage array, have components which stand off far enough to make electrical contact with the back of the adjacent card if they are not perpendicular to the board surface. Note that the *Solid Logic Technology, Packaging, Tools, and Wiring Change Procedure, Field Engineering Manual of Instruction,* Form 223-2800 gives details of card extraction tools and their use.

Tape Cable Changing

For tape cable changing, simply pull out or plug in. After a tape cable change, ensure that the new cable is correctly routed and secured in the routing with the rubber links provided. In the case of board-to-board tape cables, no routing is necessary.

Power Cable Changing

Power cable ends can be soldered, ring terminals, or plugs. Connect and disconnect the power cable ends using the instructions supplied with each change.

Wire Wrap Changing

Follow the instructions in the *Solid Logic Technology Packaging, Tools, and Wiring Change Procedure, Field Engineering Manual of Instruction,* Form 223-2800.

Console

Internal Panel Meter Changing

To change the meter, remove the two rear terminal connections, remove the two securing screws that hold the meter to the two spring leaves (one on either side) and pull the meter out from the front.

Customer/CE Usage Meter

Customer Position: Connect an oscilloscope to pin A-D3E7B02 (−Meter on) ALD KH171. This point should be in the down state under these conditions:

1. The CPU is performing useful operations and executing instructions.
2. Any device attached to the multiplex channel or either selector channel is performing useful operations (reading cards, punching cards, printing) while running on line. The same point should be at the "up" level under these conditions:
1. CPU in "wait" state and no system I/O device is operating on-line.
2. CPU in "man stop" state and no system I/O device is operating on-line.
3. CPU in "load" state and no system I/O device is operating on-line.
4. The CPU clock is not running, that is, single cycle mode (hardstop).

CE Position: Switch the CE panel key to the CE position. Check that, in this position, the CE meter runs while CPU power is on.

Both Positions: The accuracy should be checked using the meter test deck F38F, P/N 5395607. Select each position in turn and run for a time interval. Compare the meter reading at the end of the interval with the chronometer reading. The meter reads in hours and tenths of an hour. A longer time interval gives a more accurate check.

If any error is found on either meter, it must be changed. Before changing, make sure that the frequency rating printed on the meter agrees with the line frequency of the installation.

Customer/CE Usage Meter Changing

1. Swing open the main console.
2. Unsolder the circuit connections from the two terminal studs of the meter concerned.
3. Hold the meter and unscrew the two retaining screws, one on each side of the meter.
4. Remove the meter. Each meter is a sealed unit and, if defective, must be changed.

Lamp Changing

1. Remove the transparent plastic cap on the front of the indicator. The plastic capsule and enclosed bulb come out together.
2. Remove the bulb base to extract it from the capsule.
3. Reverse the procedure for replacement.

Silicon Controlled Rectifier (SCR) Changing

1. Remove the spring clamp from the back of the lamp socket. (The SCR is held by the spring clamp.)
2. Remove the plastic sleeve connectors from the SCR.
3. Remove the connecting wire from the SCR to the lamp socket. This wire is held in the lamp socket under pressure. To release the pressure, push against the wire terminal through the hole in the side of the lamp socket and pull on the wire at the same time.
4. Reverse the procedure for replacement. When replacing the plastic connectors, push on the wire going into the connector to keep the wire firmly secured within the connector.

Switch Removal Procedures

This section discusses only console switches. Power switches are discussed in "Power Supplies." See Figure 91.

Pushbuttons

1. Remove the plastic button.
2. Open the main console and unsolder the leads from the defective button.
3. Loosen the rear locking nut.
4. Twist the pushbutton counterclockwise; it unscrews from the frame and can be removed for repair or replacement.

Panel B

EPO Pullswitch:

1. Swing open the console.
2. Release the Allen screw that holds the locking disk to the switch shaft.
3. Remove the four wire terminals.
4. Remove the two switch locking nuts. Remove the switch.

Panel C

1. Remove the rotary switch knobs.
2. Unscrew the key switch plastic levers.
3. Swing open the console.
4. Remove the two bottom and two side screws that secure the panel.
5. Loosen the two top screws.
6. Slide the panel assembly downwards and outwards. The panel comes away from the console frame.
7. Unsolder the wires and unscrew the defective key or rotary switch.

Panel D

Display and Store/Display Roller Switches: The wafer and roller switch can be removed separately:

1. To remove the wafer, loosen the Allen screw that holds the control knob and take off the knob.
2. Unsolder the wafer wires and remove the two (top and bottom) wafer securing screws.
3. Extract the wafer, using the slot provided in the roller assembly.
4. To remove the roller, unplug all external wires from the terminal blocks, if they are mounted.
5. Remove the four securing screws, two at each end. Remove the roller, using the slot provided.

Display and Store Keys: All three display and store keys are mounted on one rear panel.

1. Remove the plastic key levers.
2. Swing open the console.
3. Unscrew the three vertical panel securing screws.
4. Lift out the panel assembly.
5. Unsolder the wires and remove the defective switch.

Panel F

Data and Address Keys:

1. Unscrew the plastic key levers.
2. Swing open the console.
3. Unscrew the four screws securing the panel concerned.
4. Lift out the panel assembly.
5. Unsolder the wires and remove the defective key.

Panel G

Rotary Switches and Pushbuttons:

1. Remove all the knobs and pushbuttons.
2. Swing open the console.
3. Remove the four panel securing screws.
4. Lift out the panel assembly.
5. Unsolder the wires and remove the defective switch.

Panel H

Rotary Switches and Pushbuttons: The procedure is the same as under "Panel G."

Internal CE Panel

Rotary Switch, Pushbuttons, and Potentiometers:

1. For the rotary switch, loosen the knob securing Allen screw.
2. Remove the knob.
3. Remove the switch securing nut and pull the switch out of the rear of the panel.
4. For all the other components, remove the locking nut and pull the component out to the rear.

CPU Timing Clock

Delay Line Tap Adjustments

The delay line provides an 80-nanosecond delay but it is not adjustable. In case of clock faults, the card concerned must be changed.

Dual/Multi-System Emergency Power Off (EPO)

DANGER

In a dual system or multi-system complex, the EPO switch on any CPU must remove power from all interconnected system CPUS and all shared units. When a system is isolated, all remaining systems and I/O units must have a common emergency-power-off network. Use only the following procedures to disconnect a CPU from the EPO network.

Dual System CPU Isolation

1. Remove power from both systems.
2. Remove the EPO cable from socket J3 of the CPU that is not being isolated and replace it with a dummy plug, jumpered in positions 3 and 4.
3. Remove EPO cables connecting shared I/O units and the CPU that is being isolated at the I/O units and replace them with dummy plugs. Power can now be brought up on the remaining system.

When repairs are completed, re-establish a common EPO network by replacing all EPO cables.

Multi-System CPU Isolation

1. Drop power on the system to be isolated.
2. Disconnect all CPU to I/O unit EPO cables of units shared by the processing unit; this allows any EPO switch except the one on the isolated CPU to control the shared unit.
3. Activate the bypass switch.
4. Disconnect the EPO cable between the isolated CPU and the multi-system EPO box.
5. Insert a dummy plug, jumpered between positions 5 and 6, to bypass the isolated CPU.
6. Deactivate the bypass switch immediately.

When the isolated CPU is returned to the EPO network, a similar procedure must be used to minimize the time that the bypass switch is active. Additional EPO information is in the System Reference Library, *Original Equipment Manufacturers' Information, IBM System/360 Power Control Interface,* Form A22-6906.

Hold-Out Singleshot

A variable singleshot in each channel allows the adjustment of the time between consecutive hold-out tags. These singleshots must be checked and adjusted, if necessary, for the following situations:

1. Installation of EC255286, ECA#222.
2. Installation of a CPU with EC255286.
3. A control unit added to (or deleted from) the system.
4. Cable length is changed on any channel.

Multiplex Channel: Execute a TIO to the device with the lowest priority (usually the 1052). Adjust the upper potentiometer on 01A-A1E7 for a negative pulse 3.64 microseconds ± 50 nanoseconds wide at the 50 percent point. Scope pin 01A-A1E7B02 (ALD page FB009, Note 1).

Selector Channel 1: Execute a TIO to any device on the channel and adjust the upper potentiometer on 01B-D3L7 for a negative pulse 3.65 microseconds ± 50 nanoseconds wide at the 50 percent point. Scope pin 01B-D3L7B02 (ALD page GG511, Note 1).

Selector Channel 2: Execute a TIO to any device on the channel and adjust the upper potentiometer on 01B-B1M7 for a negative pulse 3.65 microseconds ± 50 nanoseconds wide at the 50 percent point. Scope pin 01B-B1M7B02 (ALD page HG511, Note 1).

Power Supplies

This section describes power supply checks, adjustments, and troubleshooting procedures. Instructional material concerning operation and sequencing may be found in the *Power Supplies, Features, and Appendix, Field Engineering Manual of Instruction,* Form 223-2845. The *Field Engineering Manual of Instruction, Solid Logic Technology Power Supplies,* Form 223-2799, describes the theory of operation of the following types of power supplies:

High Frequency (2.5 KC)
5 KC Switching Regulator
Medium Power Standard (MPS)
Middle Power Package (Mid-Pac)
Universal Series Regulator (USR)

The IBM System/360 2040 Processing Unit uses two types of power supplies. Mid-Pac is generally used, but High Frequency (2.5 KC), is used with the lower serial numbers.

Some figure references for the Mid-Pac power supply in this manual are:

Figure 79	Power On Sequence and Timing Chart
Figure 79.1	Mid-Pac Power Off Sequence
Figure 80	Power On Sequence
Figure 81	Mid-Pac Power Supply Reference Data
Figure 92	Mid-Pac Power Supply Unit
Figure 93	Mid-Pac Power Supply Diagram
Figure 84	Mid-Pac Terminal Board Locations
Figure 11	Internal CE Panel (Mid-Pac)

Some figure references for the High Frequency power supply in this manual are:

Figure 82	Power On Sequence and Timing Chart
Figure 82.1	HF Power Off Sequence
Figure 83	High Frequency (2.5 kc) Power Supply Reference Data
Figures 94, 95	HF Power Supply Unit
Figure 85	HF Terminal Board Locations
Figure 96	Wall Frame HF Power Supply
Figure 12	Internal CE Panel (HF)

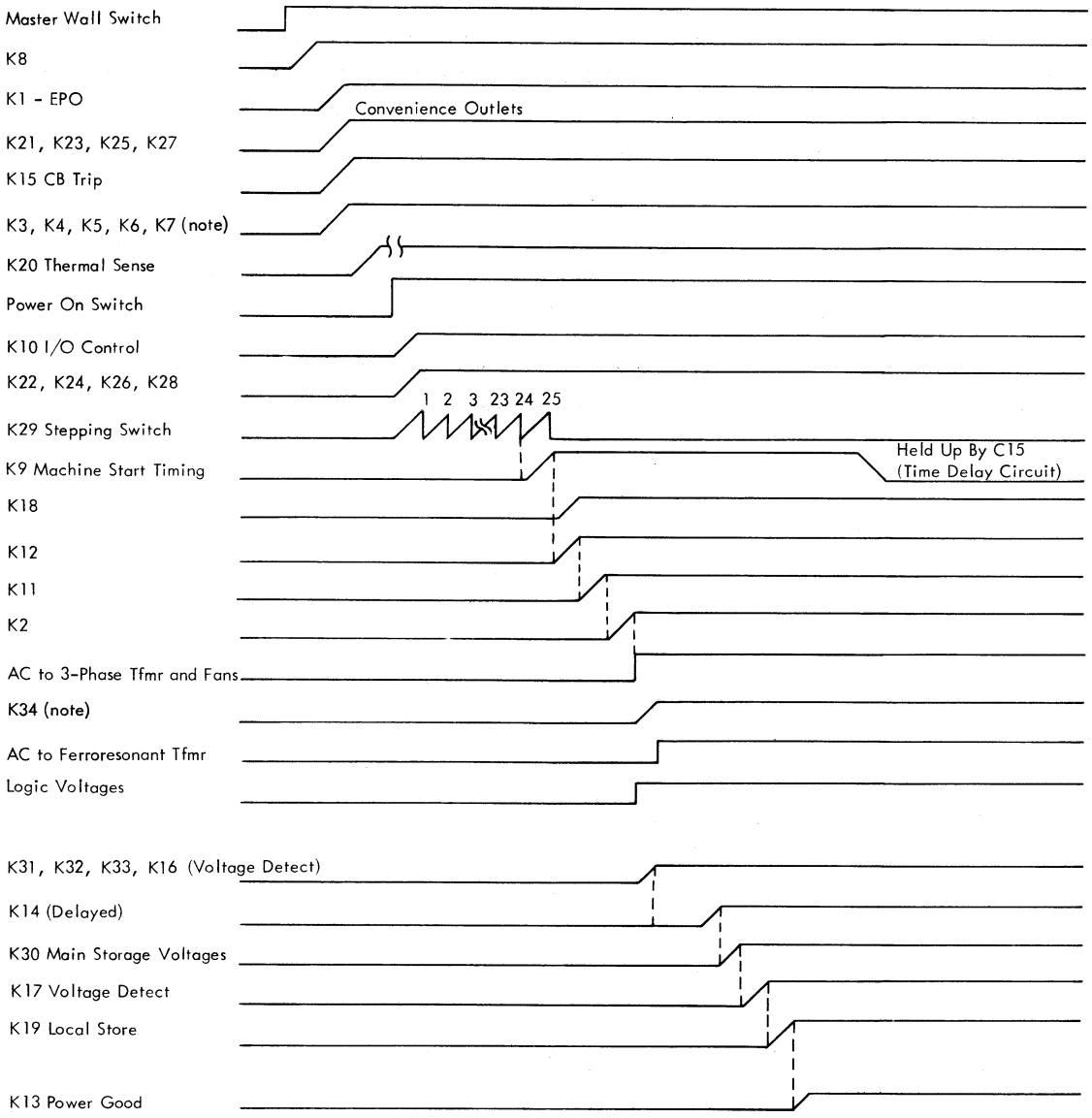
Additional information may be found in the *System/360 Model 40, 2040 Processing Unit, Field Engineering Diagrams Manual,* Form Y22-2842. Figure references for this information are:

Figure 510	Mid-Pac Power Supply Wiring Diagram
Figure 917	Mid-Pac Power Supply (MAP)
Figure 511	2.5 kc HF Power Supply Wiring Diagram
Figure 918	2.5 kc HF Power Supply (MAP)

Checks

CB Contacts

To check the contacts of a circuit breaker (CB), a meter must be used and contact resistance must be measured. The contacts are not visible, as the CB is a sealed unit. If any contacts are defective, use the removal procedure described in "CB's" to remove and to replace the CB.



Note: Contactors K3, K4, K5, K6, K7 and K34 have been removed in the revised Mid-Pac power supply (EC255055). See Figure 80.

Figure 79. Mid-Pac Power On Sequence and Timing Chart

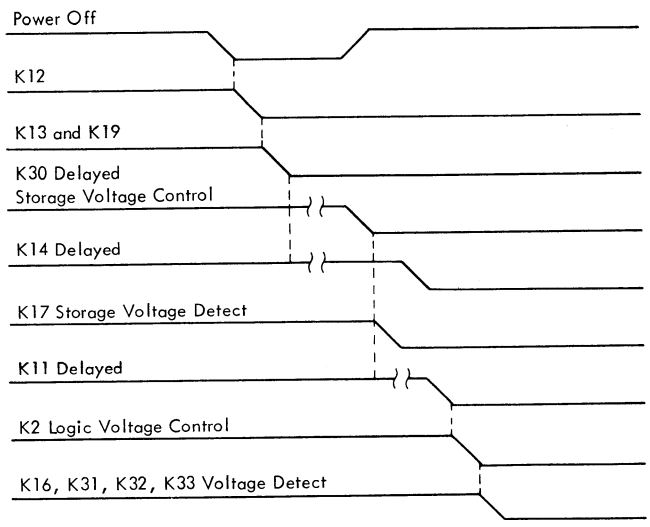


Figure 79.1. Mid-Pac Power Off Sequence and Timing Chart

Contactor Contacts

To check the contacts, use the removal procedure described in "Contactors." When the contactor is exposed, inspect and clean the contacts.

Relay Contacts

Power supplies use three types of relays:

1. Small reed-type relays are mounted on SMS cards. They are used for very low current circuit switching. It is not normally possible to service these relays, and if one is suspected, the relay should be changed. (See "Relays," and "SMS Cards.") It is not recommended that the customer engineer repair reed relays.

2. Medium size enclosed relays are individually mounted. These relays are used for power on/off and I/O sequencing. They are capable of being serviced but will normally be replaced. The contacts are visible through the plastic cover. To clean the contacts, remove the spring-retaining clip, remove the relay and lever off the plastic protection cover to expose the contacts.

3. Large "Duo" type relays are individually mounted. These relays are used only for heavy-current circuits, and one relay is used in the CPU frame for the control alarm within the IBM 1052. This type of relay is fully exposed for servicing of contacts.

Stepping Switch Contacts

The stepping switch is used for I/O power sequencing. It consists of three banks of 26 contacts and four magnet control contacts. It is mounted behind the I/O connectors and the whole subpanel must be removed for access. "Stepping Switch" describes the removal procedure. After the subpanel is removed, the stepping switch can be checked without removing any other covers.

Manually operate the stepping switch and check the following points:

1. The magnet control contact should break just after the ratchet-winding cam has moved into the next ratchet tooth.

2. The three switch wafers should move forward one complete contact for every operation of the ratchet mechanism, so that the contacts always mate fully and never overlap.

3. All contacts should be clean.

NOTE: If any adjustments are necessary, use the procedures outlined in "Stepping Switch."

Mid-Pac Power Supply Adjustments

CAUTION

Power supplies *must* be adjusted in the prescribed order to prevent machine damage, which results in loss of machine time and costly repairs.

Use the internal CE panel meter to set the voltage levels. Check these settings with a voltmeter (Branch Office tool, P/N 461079) and calibrate the CE meter accordingly. *Never* increase the output of the supply beyond its overvoltage limit.

Use these procedures for adjustment of the power supplies (modules).

POWER SUPPLY	OUTPUT ADJUSTMENTS	OVERVOLTAGE ADJUSTMENT
−3v	1	4
+3v	1	4
−6/−9v	2	none
+6v	1	4
+6Mv	3	5
+18v	1	4
+48v	1	none
+60XYv	3	5
+60Zv	3	5

NOTE: The +48v power supply is not regulated on machines with the revised Mid-Pac power supply (EC255055).

Procedure 1

Adjust potentiometer on SMS amplifier card to set output level of the power supply.

1. Measure and monitor the output voltage at the CE panel for the applicable power supply:

Wall plug

CB 1 made

Power to 23v supply

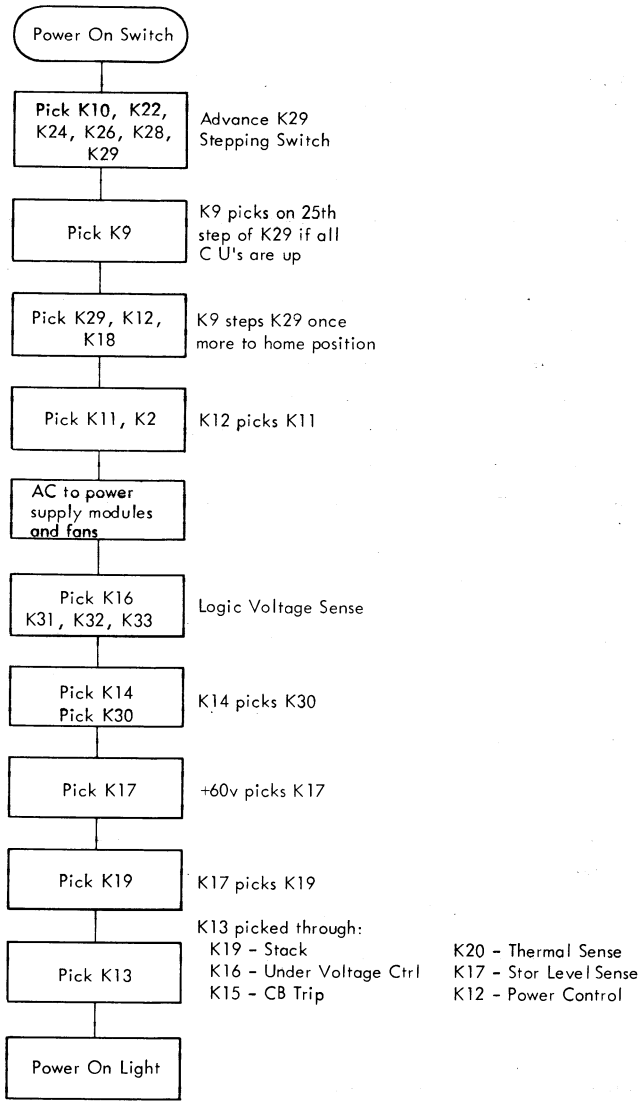
Power K8 through EPO switch closed
Pick K1
CB 6 made-Convenience outlets have power

Pick K21, K23, K25, K27-EPO Relays

Pick K15 through K8 n/o point and power supply CB n/c points in series

Pick K3, K4, K5, K6, K7 through associated thermal points and K18 n/c (See note)

Pick K20 through K3, K4, K5, K6, K7 n/o points in series (See note)



Note: Pick K20 through associated thermals and K18 n/c in revised Mid-Pac power supply.

Figure 80. Mid-Pac Power On Sequence

POWER SUPPLY	ALTERNATE TEST POINT	ALD PAGE
−3v	ROS TB1-9, 10	YC162
+3v	PS TB1-5, 8	YC161
+6v	ROS TB1-11, 12	YC162
+18v	MS TB1-9, 10	YC162
+48v	PS TB1-4, 6	YC171

NOTE: The +48v power supply cannot be adjusted on machines with the revised Mid-Pac power supply (EC255055).

2. Vary the red knurled knob of the potentiometer on the SMS amplifier card until the meter reads the specified voltage.

Procedure 2

Adjust the external potentiometer to set the output level of the power supply.

1. Measure and monitor the output voltage at the CE panel for the applicable power supply:

POWER SUPPLY	ALTERNATE TEST POINT	ALD PAGE
−6/−9v	Gate A, TB1-5, 6	YC162

2. Adjust the external potentiometer to give the required voltage output.

Procedure 3

Adjust the potentiometer on the SMS amplifier card in combination with the external potentiometer (on the external CE panel) to set the output level of the supply. The external potentiometer is ganged to an external variable transformer.

1. Measure and monitor the output voltage at the CE panel for the applicable power supply:

POWER SUPPLY	RANGE	ALTERNATE TEST POINT	ALD PAGE
+6M	+4 to +7	PS TB1-5, 6	YC161
+60XY	48 to 66	MS TB1-1, 2	YC162
+60Z	+48 to +66	MS TB1-11, 12	YC162

2. Record the voltage before starting adjustments, so that the power supply may be reset to this value.

3. Adjust the potentiometer on the internal CE panel for maximum voltage, and the potentiometer on the SMS amplifier card to reach the upper range of the applicable power supply.

4. Reset the potentiometer on the internal CE panel to give the voltage recorded in step 2.

Procedure 4

Adjust the potentiometer on the SMS overvoltage card to set the output level of the power supply to trip CB1 of the applicable supply.

1. Measure and monitor the output voltage at the CE panel for the applicable power supply:

POWER SUPPLY	ALD	OVERVOLTAGE LIMIT
−3v	YC161	See Figure 81
+3v	YC161	
+6v	YC161	
+18v	YC161	

Volts	Amps	Overvolts Max	Undervolts Min	Adj Range	Assembly P/N	Schematic P/N	SMS Amplifier Card P/N	Overvoltage Card P/N
-3v	30a	3.8v ± 0.4v			5392884	5392885	374873	372677
+3v	45a	3.9v ± 0.4v			5392896	5392897	374873	372677
-6/-9v	6a	none			5392888	5392889	374885	none
+6v	24a	6.7v ± 0.3v	5.2v ± 0.1		730490	730491	372990	372423
+6 MV	32a	7.8v ± 0.8v		+4 to +7	5392880	5392881	374871	374875
+18v	7a	21.0v ± 0.2v			5392886	5392887	374872	374874
+48v	1a	none			5392890*	5392891*	374886*	none*
+60 XYV	1a	67.5v ± 0.5v		+48 to +66	5392892	5392893	374887	374876
+60 ZV	4a	67.5v ± 0.5v		+48 to +66	5392894	5392895	374887	374876
TROS				See TROS				
LS VM				See Figure 64				
LS VXY				See Figure 65				
SP VXY				See Figure 68				

*These part numbers do not apply to the revised Mid-Pac power supply (EC255055); its assembly part number is 5392999.

Figure 81. Mid-Pac Power Supply Reference Data

2. Adjust the red knurled potentiometer on the SMS amplifier card to the overvoltage limit for the applicable supply. If the CB trips before the overvoltage limit is reached, turn the screwdriver-adjust potentiometer on the SMS overvoltage card counterclockwise so that the adjustment of the red knurled potentiometer on the SMS amplifier card allows the overvoltage limit to be reached.

NOTE: If the +3v supply drops overcurrent before overvoltage, disconnect the laminar bus from four boards and check that overvoltage drops power at specified setting.

3. When the overvoltage limit is reached, slowly turn the screwdriver-adjust potentiometer on the SMS overvoltage card clockwise until the CB trips.

4. Set +6v supply to 5.2v and slowly adjust knurled knob of potentiometer R-23 on the undervoltage unit (Figure 93) until K16 drops and power sequences down. Turning the potentiometer counterclockwise lowers the trip point. After adjusting, return the +6v supply to nominal setting.

5. Readjust the voltage level of the supply, using Procedure 1.

Procedure 5

Adjust the potentiometer on the SMS overvoltage card to set the output level of the power supply to trip CB1 of the applicable supply.

1. Measure and monitor the output voltage at the CE panel for the applicable power supply:

POWER SUPPLY	ALD	OVERVOLTAGE LIMIT
+6M	YC161	See Figure 81
+60XY	YC171	
+60Z	YC171	

2. Record the voltage before starting adjustments, so that the power supply may be reset to this value.

3. Slowly turn the screwdriver-adjust potentiometer for the applicable supply on the internal CE panel clockwise to bring the voltage output to the overvoltage upper limit. If the CB trips before this limit is reached, turn the screwdriver-adjust potentiometer on the SMS overvoltage card clockwise and repeat this step.

4. Adjust the screwdriver-adjust potentiometer on the SMS overvoltage card counterclockwise to trip the CB.

5. Reset the screwdriver-adjust potentiometer for the applicable supply on the internal CE panel to the value recorded in step 2 above.

Wall Frame Mid-Pac Power Supply Adjustments

The foregoing procedures apply to wall frame Mid-Pac power supplies as well as to conventional Mid-Pac supplies.

HF Power Supply Adjustments

This section describes the major power supply adjustments.

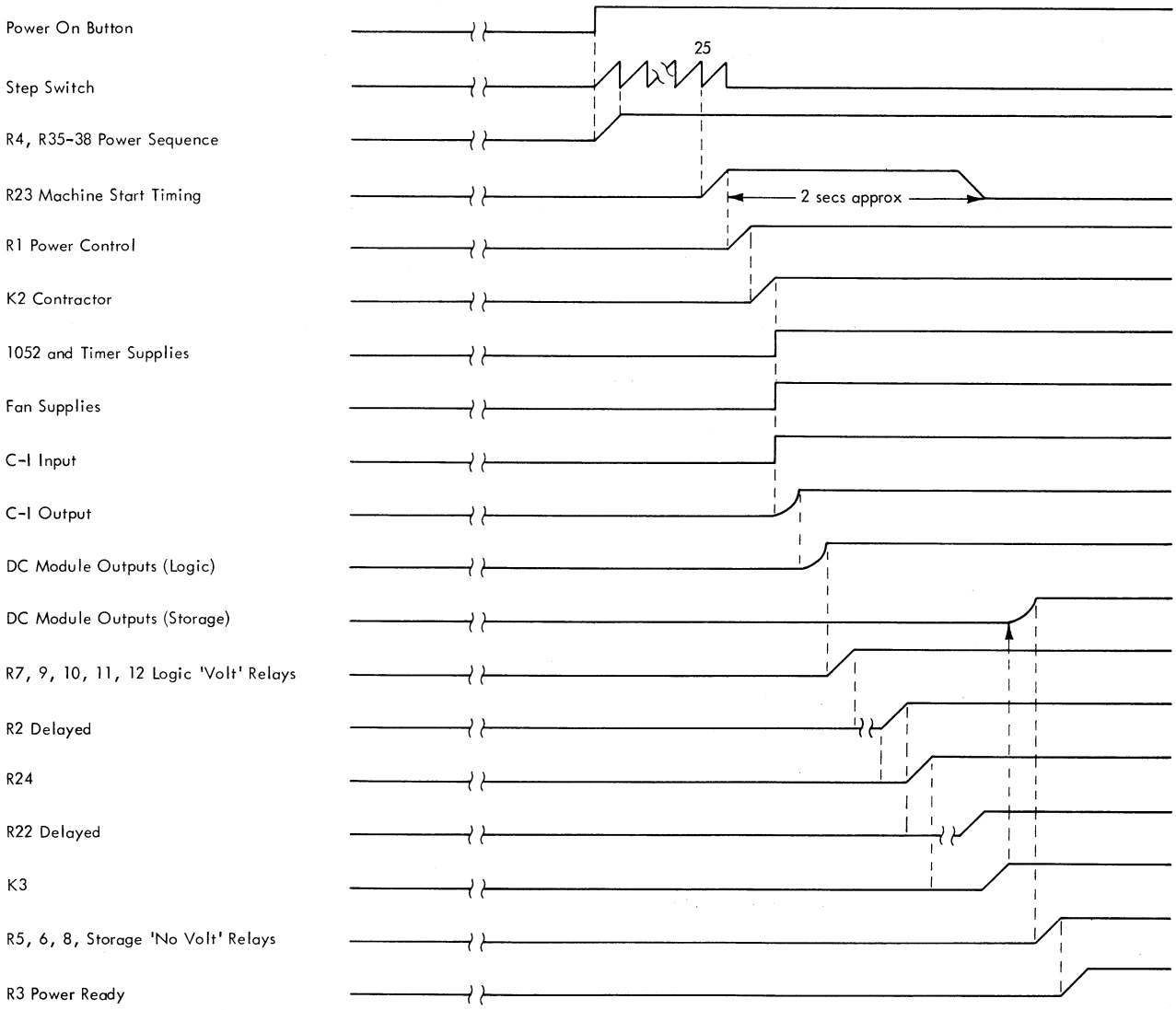


Figure 82. HF Power On Sequence and Timing Chart

Voltages and Current (Figure 12)

Adjustment of the +6v, 25A supply will change the operating point of local storage and storage protect. You must check both using the marginal check procedure.

The +48v supply is positioned at the console end of the main frame.

–3v:

1. Remove the power supply top safety cover ("All Modules Except 24v" section). This exposes the HF modules and potentiometers.

2. Select the –3v module (top left) and use the potentiometer mounted on the outside edge of one of the two SMS cards to make any necessary voltage adjustments.

3. If the voltage ripple exceeds 100 mv, change either the whole module or the filter capacitors within the module.

4. After components have been changed, the supply may have to be readjusted.

+3v: The setting-up procedure is the same as that for –3v except that the test probes must be reversed.

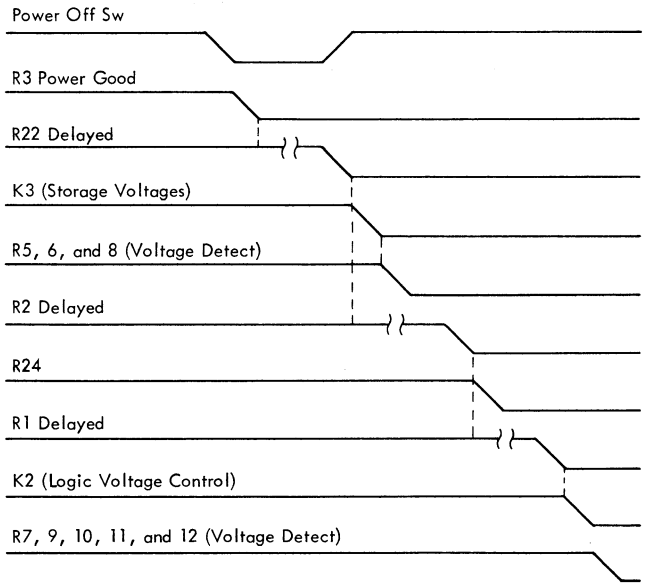


Figure 82.1. Power Off Sequence and Timing Chart

The +3v module is positioned below the –3v module.

+6v @ 25A: The setting-up procedure is the same as that for +3v. The +6v module is positioned at the bottom right. Any adjustments of this voltage affect the settings of LS/Vxy and PS/Vxy. Therefore, after the +6v, 25A has been changed, the local storage and storage protect marginal checking procedures should be executed. See "Local Storage" and "Storage Protect."

+18v: The setting-up procedure is the same as that for +3v. This module is positioned to the right of the –3v module.

+24v: The I/O power sockets must be removed to provide access to the +24v components (see "I/O Power Socket Module"). The setting-up procedure is

Volts	Amps	Overvolts Max	Undervolts Min	Adj Range	Assembly P/N	Schematic P/N	SMS Amplifier Card P/N	SMS Overvoltage Card P/N
-3v	40a			-2.97 to -3.45	5261220	5261221	372966	372973
+3v	40a			2.97 to 3.45	5261220	5261221	372966	372973
+6v	25a			5.94 to 6.6	5261230	5261231	372966	372973
+6 MCV	40a			3.94 to 7.6	5261240	5261241	372975	372973
-6/-9v	4/6a			-5.3 to -10.0	5261300	5261301	372972	372973
+18v	5a			17.82 to 18.6	5261270	5261271	372967	372973
+60 XYV	1a			47.4 to 66.6	5261260	5261261	372970	372973
+56 ZV	4a			47.4 to 66.6	5261480	5261481	374771	372973
TROS				+66ma				
LS VM				-6.96v				
LS VXY				+2.25				
SP VXY				+4.7v				

Figure 83. High Frequency (2.5 kc) Power Supply Reference Data

the same as that for +3v. Note that the components are mounted behind the I/O power sockets and are not modular in construction.

+48v: This module is inside the console end of the main frame and is accessible from the same side as the main storage logic. The module is permanently exposed, and the setting-up procedure is the same as that for +3v.

+6vm: The setting-up procedure is the same as that for +3v. The module is positioned to the right of the +3v module.

+220v: This voltage is used for fans and the converter inverter input. This voltage is fixed by tappings on transformer 3. It has no continuously variable adjustment, but the transformer input tappings should be adjusted to give a 220v output between any two phases. This is factory-adjusted and needs alteration only if the local installation voltage changes (for example, a field transferred system).

Convenience Outlets

Machines wired to 50 cycle supplies have 220 VAC convenience outlets. Machines wired to 60 cycles have 110 VAC receptacles.

Overvoltage

Two customer engineers are needed to adjust the overvoltage unit, which is at the top left of the power supply. The internal CE panel meter is accurate enough for this operation and no test equipment is necessary.

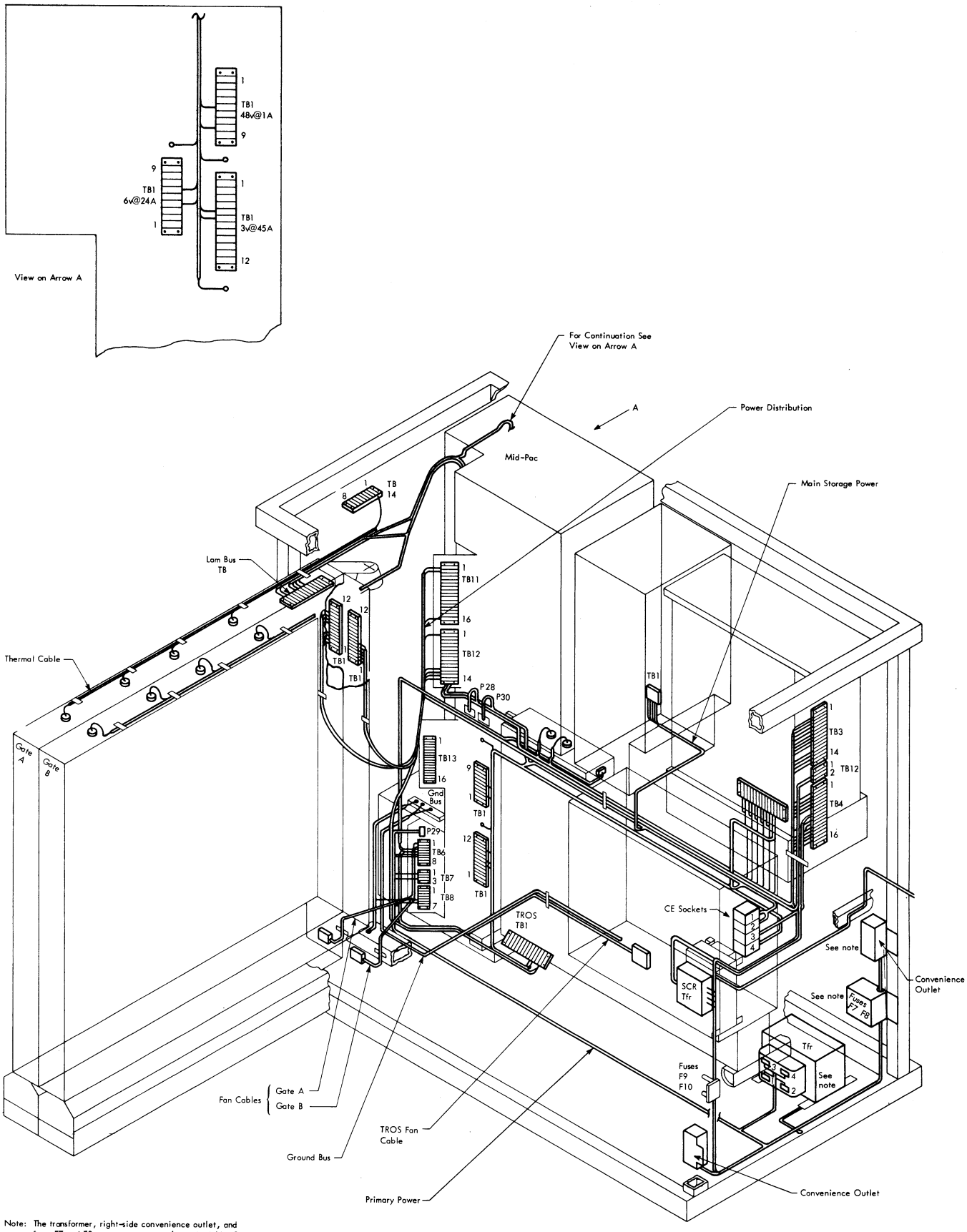
+3v Supply:

1. Remove the safety cover from the HF module.
2. Switch the select voltage switch on the internal CE panel to the +3v position and note the meter reading.
3. One CE should watch the internal panel meter while the other increases the +3v supply, using the potentiometer on the +3v HF module. The overvoltage circuits should trip at +4.5v and power sequences down.
4. If the overvoltage circuits trip before +4.5v, turn the +3v potentiometer on the overvoltage unit (R4) to maximum (counterclockwise direction).
5. Return power to the system and restart.
6. If the overvoltage circuits do not trip at 4.5v, leave the +3v HF module potentiometer set so that the meter reads 4.5v.
7. Adjust the +3v potentiometer on the overvoltage unit (R4) until the overvoltage circuits trip and system power drops.
8. Mark this setting of the overvoltage potentiometer and return the +3 VDC to the original value.

The above procedure should be repeated for these DC supplies:

–3v Supply: For the –3v supply, set the –3v potentiometer on the overvoltage unit (R7) so that power drops at –4.5v.

+6v Supply: For the +6v supply, set the +6v potentiometer on the overvoltage unit (R9) so that



Note: The transformer, right-side convenience outlet, and fuses F7 and F8 are not present on the revised Mid-Pac **power supply (EC255055).**

Figure 84. Mid-Pac Terminal Board Locations

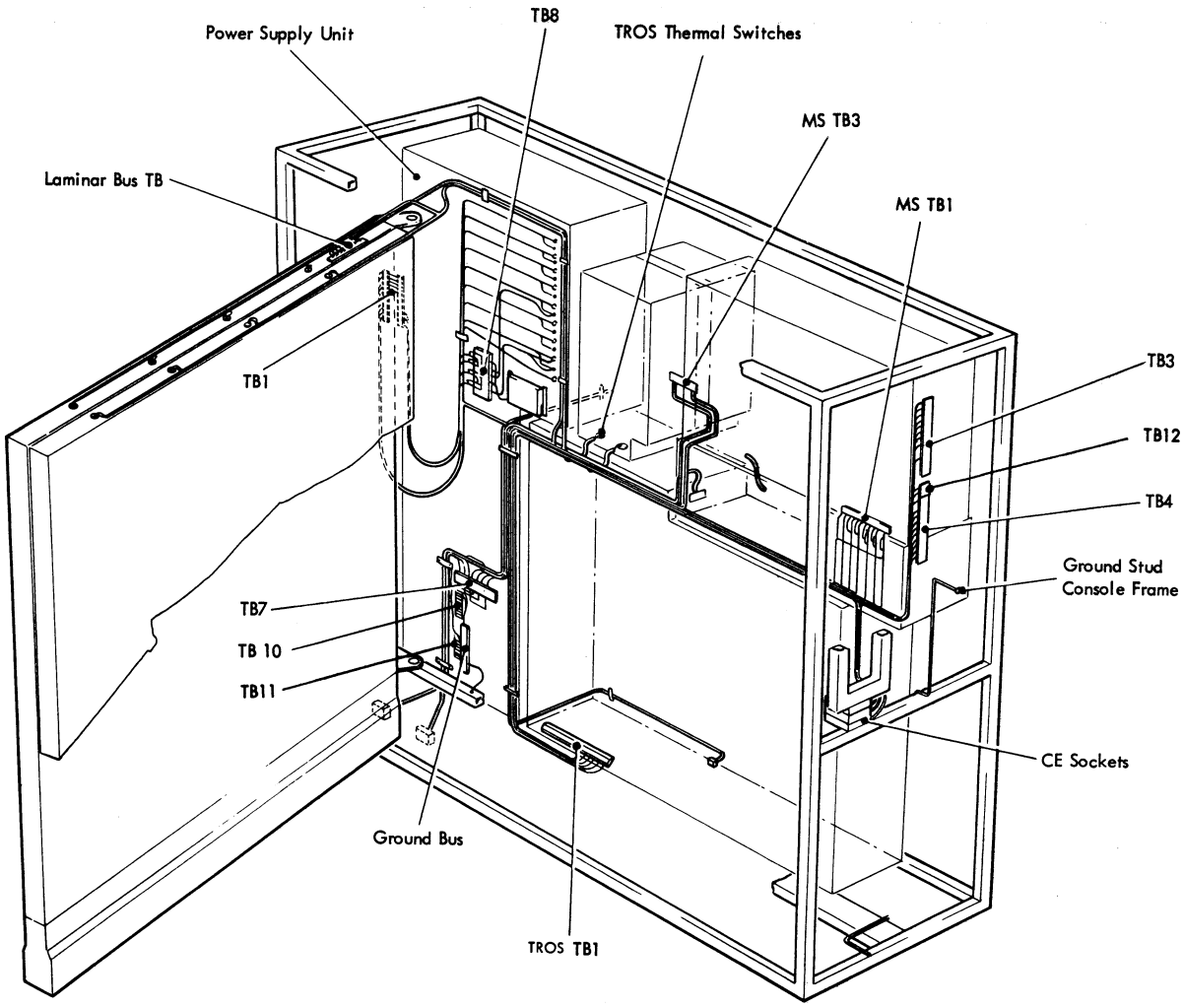


Figure 85. HF Terminal Board Locations

power drops at +8.0v; and set the undervoltage potentiometer (R12 same unit) so that the undervoltage circuits trip at +5.2v.

+6M Supply

For the +6M supply, set the +6v potentiometer on the overvoltage unit (R9) so that power drops at +8.0v.

+56Z and +60 XY Supplies: For the +56Z and +60 XY supplies, set the +6v potentiometer on the overvoltage unit (R9) so that power drops at +70.0v in both cases.

+18v Supply: For the +18v supply, set the +6v potentiometer on the overvoltage unit (R9) so that power drops at +22.0v.

+6v Potentiometer (R9): R9 is the general overvoltage potentiometer for the +6v, +6 VM, +60 VXY, +60 VZ and +18v. It should be adjusted for each DC supply and after all have been tested, set to the midpoint between the most extreme readings.

Additional Adjustments for 60v and 18v Supplies

If difficulty is experienced in adjusting the 60v and 18v supplies, then the three voltage divider potentiometers R37, R39, and R42 may need adjustment. The overvoltage PNP transistors need an emitter voltage of +6v.

R37 taps +6v off a voltage divider across the 18 VDC supply.

R39 taps +6v off a voltage divider across the 18 VDC supply.

R42 taps +6v off a voltage divider across the 18 VDC supply.

1. Use a voltmeter to check that +6v is being provided to the overvoltage transistor emitters.
2. Measure the potentiometer wiper with respect to ground (supply common line).
3. If any potentiometer is not providing +6v, it must be adjusted.

In later versions of the overvoltage unit, these last three potentiometers are inside the unit, and the unit front panel (hinged) must be swung to the left for interior access.

Overcurrent

The overcurrent circuits for each HF module are all on an SMS card. The overcurrent SMS card is the inside card of the two cards on each module. It holds the overcurrent relay and indicator and the overcurrent circuits. The overcurrent triggering transformer winding is in a sealed block, and present construction does not allow any adjustment of the triggering circuit.

Removals and Replacement

This section describes the major module, component removals, and replacement procedures.

Converter Inverter (CI)

NOTE: Before removal, be sure that all cables are labeled for identification.

The CI is in the center of the power supply unit. The removal procedure is:

1. Switch off line supplies at the customer terminal.
2. Remove the main CI safety covers.
3. Loosen the screws on the right side of the covers.
4. Remove the screws on the left side of the covers.
5. Slide the safety covers out to the left. This exposes the CI unit.
6. Remove the capacitor that is bolted to the frame at the top right of the CI, to prevent damage by the top right corner of the CI unit when this unit is withdrawn.
7. Remove the four mounting screws along the bottom edge of the unit.
8. Remove the internal cables that connect to the terminal block on the bottom right of the unit. When removing the internal cables, if the cables are not numbered, be sure that some method of labeling is used. This will avoid wrong connections during replacement.
9. Support the unit by hand along the bottom edge. If cable looms make it difficult to support the unit, the cover can be removed (three screws) and the CE can hold the unit by the internal frame members.
10. Remove the four mounting screws along the top of the unit.
11. Lift out the unit.

More details of the CI construction and theory of operation is described in *Solid Logic Technology Power Supplies, Field Engineering Manual of Instruction*, Form 223-2799.

This material would be useful if any other components are suspected or require attention.

For fan changing procedure, see "Main Frame."

Modules

This section describes HF modules, overvoltage unit, I/O and HF power socket module.

NOTE: Be sure that all cables are numbered or labeled before removal.

Each module is secured by two screws.

All Modules Except 24v: The −3v, +3v, +60 VXY, +56 VZ, +18v, +6 VM, +6v, and −6 to −9v modules are all in the top half of the power supply unit.

The +48v (IBM 1052) module at the console end of the main frame has no covers and removal is the same as that for the other modules. The removal procedure is:

1. Switch off line supplies at the customer terminal and remove the main module safety cover.
2. Loosen the screws down the right side of the cover.
3. Remove the screws down the left side of the cover.
4. Slide the cover out to the left. This exposes the DC modules. Use the diagrams in "Locations" to identify the suspected module.
5. Remove the external cable connections from the module terminal block. Be sure that cables are numbered, or labeled, to avoid wrong connections during replacement.
6. Each module is secured by two screws, one at the top and one at the bottom; both are on the same side as the module terminal board. Support the module and remove these two screws.
7. Lift out the module.

24v Module: The +24v module is bolted to the power supply frame and is located in the bottom power supply compartment. The removal procedure is:

1. Remove the bottom compartment safety cover by loosening the right-hand mounting screw and removing the two left mounting screws.
2. The cover then slides out to the left. This exposes the bottom compartment. The +24v components are behind the main CB and indicator fuse panel.

3. Support this panel and remove the four mounting screws on the left outside the bottom compartment.

4. Lower this panel. The +24v components are now visible.

5. Remove as required. Replacement procedure is the reverse of the removal procedure.

Overvoltage Unit: This unit is at the top left of the power supply unit. The removal procedure is:

1. Switch off line supplies at the customer terminal.

2. Remove the upper power supply safety cover by loosening the screws on the right of the unit and removing the screws on the left of the unit.

3. Slide the cover out sideways.

4. If the overvoltage unit has a vertical hinge on the left side, remove the two right screws.

5. Remove the two SMS cards on the left of the unit and swing the unit open to the left.

6. Internal components can now be reached for repair or replacement.

7. If the overvoltage unit has no hinge, unplug the external wires.

8. Support the unit by hand, remove the four mounting screws, and extract the unit.

9. Replacement procedure is the reverse of the removal procedure.

I/O *Power Socket Module (Figure 92):* This module holds the I/O power sequence components.

This module is in the bottom power supply compartment at the top right. It holds the I/O power sequence sockets, the stepping switch, four EPO (Emergency Power Off) relays (31 to 34), and four I/O power sequence relays (35 to 38). The removal procedure is:

1. Switch off supplies at the customer terminal.

2. Remove the bottom compartment safety cover by loosening the right-hand screw, removing the two left-hand screws, and slide the cover out sideways.

3. Unplug the connectors from the left side of the module. Take care to number any unnumbered connectors to avoid wrong connections during replacement.

4. Support the module by hand and unscrew the four module-securing screws. These are accessible from the outside on the right of the power supply unit.

5. Replacement procedure is the reverse of the removal procedure.

Removal Procedures

ALD YA070 contains a chart of relays and contactors. The physical locations are shown on Figures 88 and 90.

60-Cycle Power Supply: CB1 is located in the bottom compartment.

1. To remove CB1, first remove the bottom compartment safety cover, then remove the six cable connections to the CB1 terminals.

2. Finally, support CB1 and remove the four securing bolts.

3. CB1 can be lifted out for exchange. It is rivet-sealed and cannot be serviced.

4. Replacement procedure is the reverse of the removal procedure.

Contactors: If contactors are dismantled, do not lose the spring located between the magnet and contact assemblies.

All contactors are basically similar in construction. They are secured to the frame by two screws, one at the top left and the other at the bottom right. Select the contactor to be inspected and remove as follows:

1. Disconnect the cables.

2. Support the contactor and remove the top left screw.

3. Loosen the bottom right screw and lift the contactor up. The bottom screw hole on the contactor is slotted.

4. Remove the contactor for repair or replacement.

5. If it is necessary to dismantle the contactor for repairs, unscrew the four main screws on the contactor body.

6. The contact assembly now lifts off the coil assembly. Ensure that the large spring coil between the two assemblies is not lost in this operation.

7. If the contact assembly must be dismantled, unscrew the two screws on the top (outside) contact bank. The contact bank (or banks) can then be dismantled.

8. Replacement procedure is the reverse of the removal procedure.

Relays: All relays except the duo type are a push fit. The three types of relays used are different in construction and are removed as follows:

1. For the small reed-type relay, select the SMS card holding the suspected relay and pull off the relay using an extractor. It is a push fit onto the pins that are soldered on the card.

2. For the medium size enclosed relays, select the suspected relay, release the securing spring clip, and pull out the relay. The relay and base are a plug and socket arrangement.

3. For the large size duo-type relays, the relay must be unscrewed from the frame.

Stepping Switch: Change this switch only when adjustment is not possible.

There is only one stepping switch used in the 2040 CPU. This is on the I/O power socket module. If stepping switch faults are diagnosed as maladjustments or bad contacts, the stepping switch should be serviced while still on the module assembly. In cases

where the stepping switch must be changed or removed, use the following procedure:

1. Extract the I/O power socket module as described in "I/O Power Socket Module." The stepping switch is on this module.
2. Be sure that all wires soldered onto the stepping switch are numbered or can be easily recognized.
3. Unsolder the wires.
4. Unscrew the two stepping switch screws.
5. Lift out the stepping switch.

SMS Cards

- **Do not disturb the SMS card potentiometers.**

Use wiring diagrams or location charts to select the suspected SMS card and pull it out. When removing SMS cards that have potentiometers mounted on them (those on the HF modules) take care not to disturb the setting of the potentiometers. If the cards are replaced after inspection, and the potentiometers have been disturbed, recheck the voltage setting procedures.

Indicators

- **The overvoltage unit indicators have a special spring-retaining clip.**

The power supply unit uses two types of indicators. Both are sealed cartridges. The small two-pin pluggable type is used for overvoltage current indications. The larger indicator is built on a fuse holder and indicates that a fuse has blown.

To remove the smaller cartridge, pull it out. Note that the overvoltage unit has two of these small indicators that are not plugged in but are held in by spring clips. To remove these, the overvoltage unit must be opened and the two "push on" wire terminals must be removed from the two pins of the cartridge. The cartridge can then be pushed out from the rear. Retain the spring clip until replacement.

To remove the larger cartridge, twist and pull. The cartridge and fuse will come out together.

Fuses

- **The main CI fuses are in a special bracket.**

Fuses on the power supply unit follow the standard pattern of twist and pull, or unscrew, except for the main CI fuses, which are fixed in a plastic bracket. The bracket is on the left of the CI unit and has a protruding handle. The bracket must be pulled out horizontally to expose the fuses.

CAUTION

Use only correct part number for replacement fuses. *Do not substitute.*

Fault Finding

To assist in diagnosing power supply faults, power MAP's (Figures 917 and 918) are provided.

Fault Areas

The CPU faults that are indicated are overheating (thermal), overcurrent, and voltage. These must be traced individually either to faulty fans or to faulty circuit components.

The main power supply areas that are not indicated are the contactor and relay contacts. Fault finding on these areas is easier if you depress the power on pushbutton and observe the voltages that are sequencing on. Start with the 24 VDC followed by any one of the logic voltages and end with the storage voltages.

Symptoms and Resolution

- **Use the power supply MAP for basic trouble shooting.**

Power Will Not Sequence On:

1. CPU: If no indicators are on, the probable fault is a relay or contactor failing to operate because of a dirty contact. If any indicators are on, this gives an immediate starting point.
2. I/O: I/O power-on sequencing is initiated by the operation of relay 3. R3-3 contacts activate the stepping switch, which starts the I/O power-on sequencing. These circuits may be checked by shorting out pins three and four of the first five I/O sockets and listening for the stepping switch skipping through these first five positions. If these circuits are proved, check that the first I/O device to be sequenced has power connected to it and has no fault in the power circuits. If no fault can be found and the device will still not sequence on, check the device-to-CPU cabling.

Power Will Not Sequence Off: This probably occurs because R23 is not dropping. Check the power-off pushbutton contacts and circuit.

The following areas of the IBM 2040 are described:

Main Frame (Figures 86, 87, 88, 89, 90)
CPU Logic Gates (Figures 86, 87)
Console (Figure 13)
TROS (Figure 90)
Main Storage
Local Storage
Storage Protect
Connectors (Figure 88)
Boards
Cards

Main Frame

See Figures 86, 87, 88, 89 and 90.

The interior of the CPU is accessible by the doors at the sides of the main frame cabinet. The console panel fitted above the table may be swung out on a hinge to give easy access and visibility during maintenance operations.

The front of the CPU is the view presented when facing the console panel.

Indicators and controls not mounted on the console panel are accessible via the side doors, without the removal of further covers. The major components packaged in the CPU are:

CPU logic gate
TROS logic and module arrays
Main Storage logic and core arrays
Power Supplies (see "Power Supplies" for detailed locations)
Internal CE Panel
Tail Gate
Mixer Panel

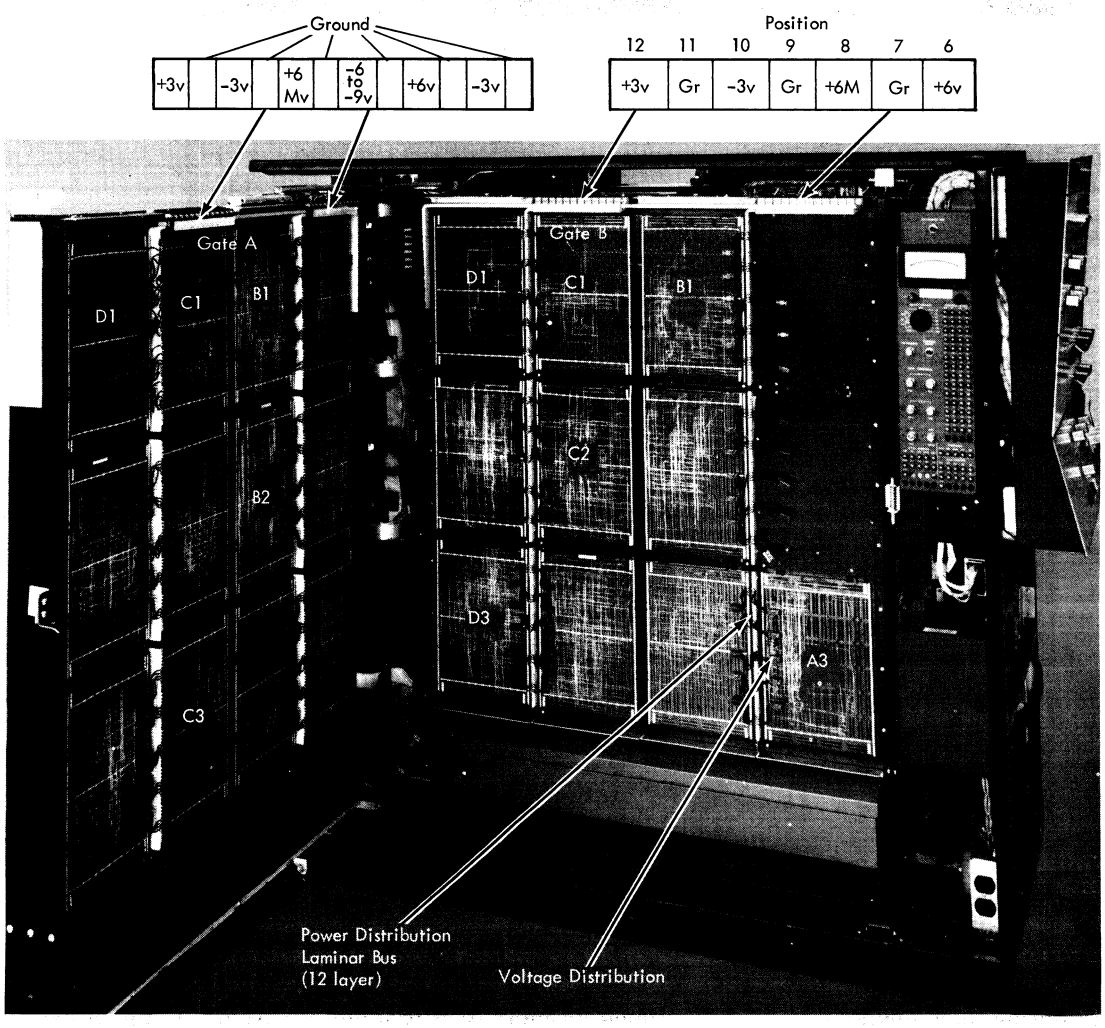


Figure 86. SLT Gates A and B

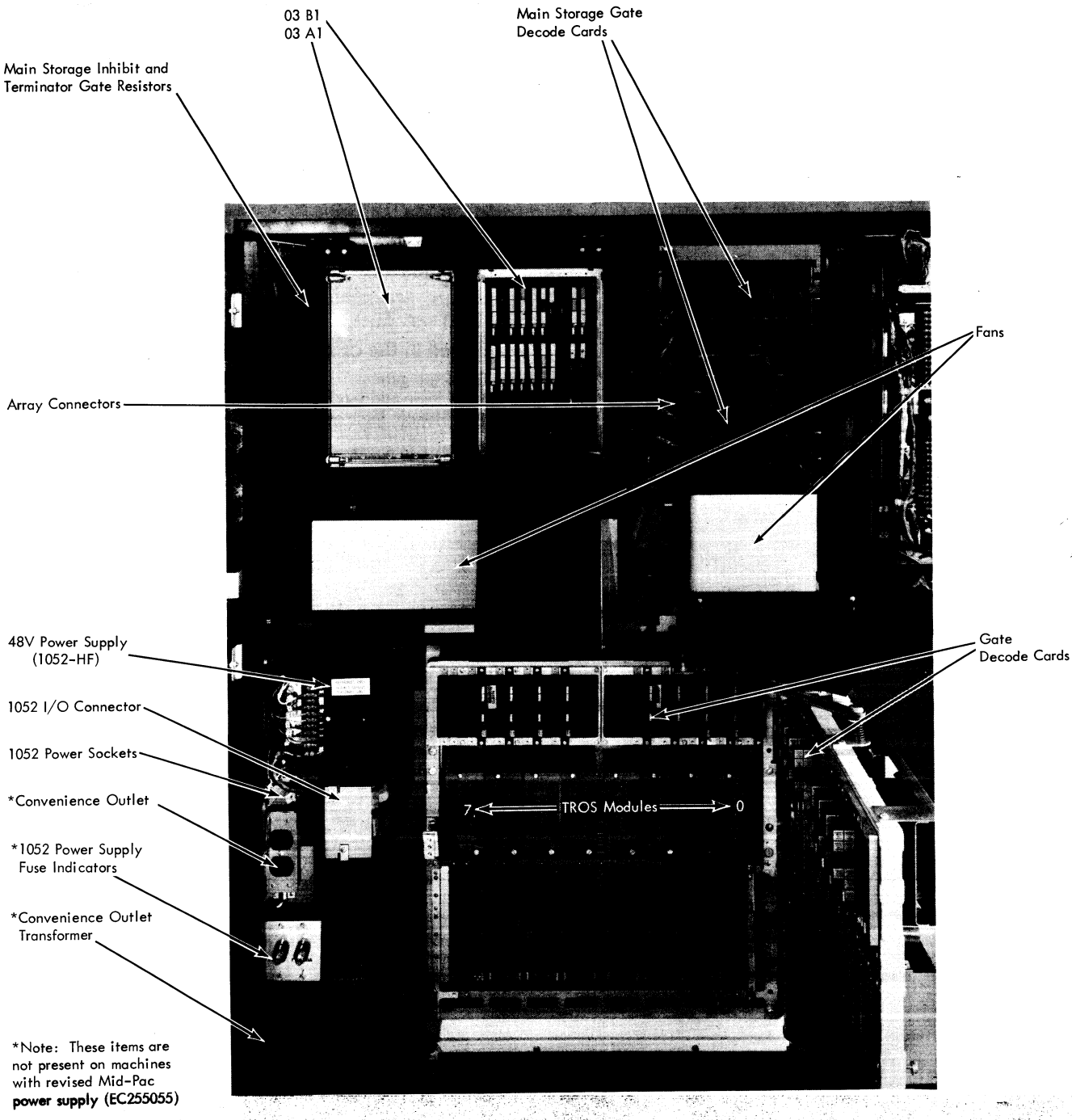


Figure 87. CPU – Right Side

CPU Logic Gates (Figures 86, 87)

The CPU logic gates, gate A and gate B, are near the left side of the main frame. They are hinged at the farthest end from the console to give maximum working space and visibility during maintenance.

Each logic gate in the 2040 contains 12 boards into which are plugged the SLT cards. The addressing scheme for the gates, boards, and SLT cards may be found under "Boards" and "SLT Cards."

SLT cards are accessible by dropping the relevant hinged board cover. These covers must not be left open for more than 10 minutes with power on, or overheating results because of improper air flow.

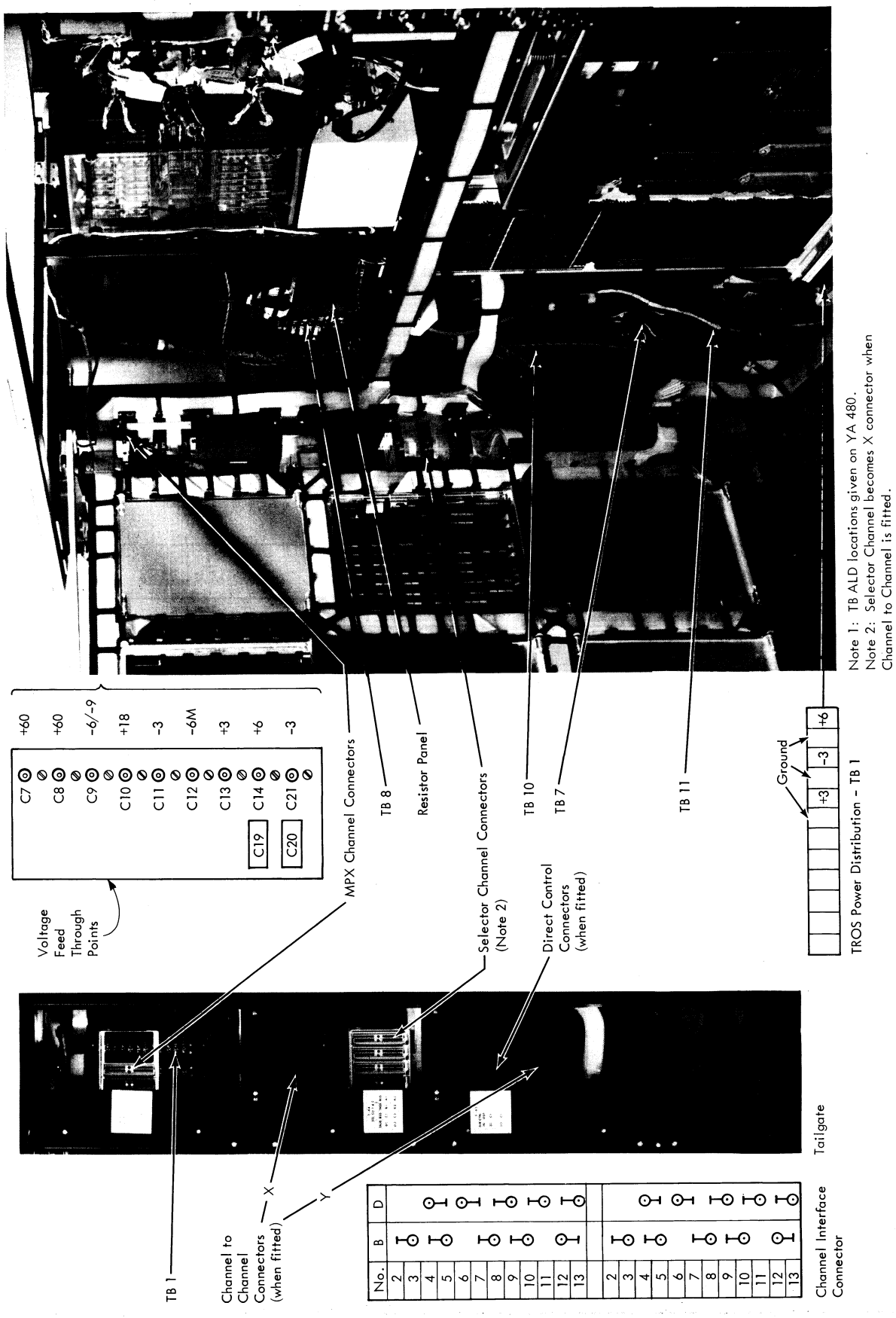
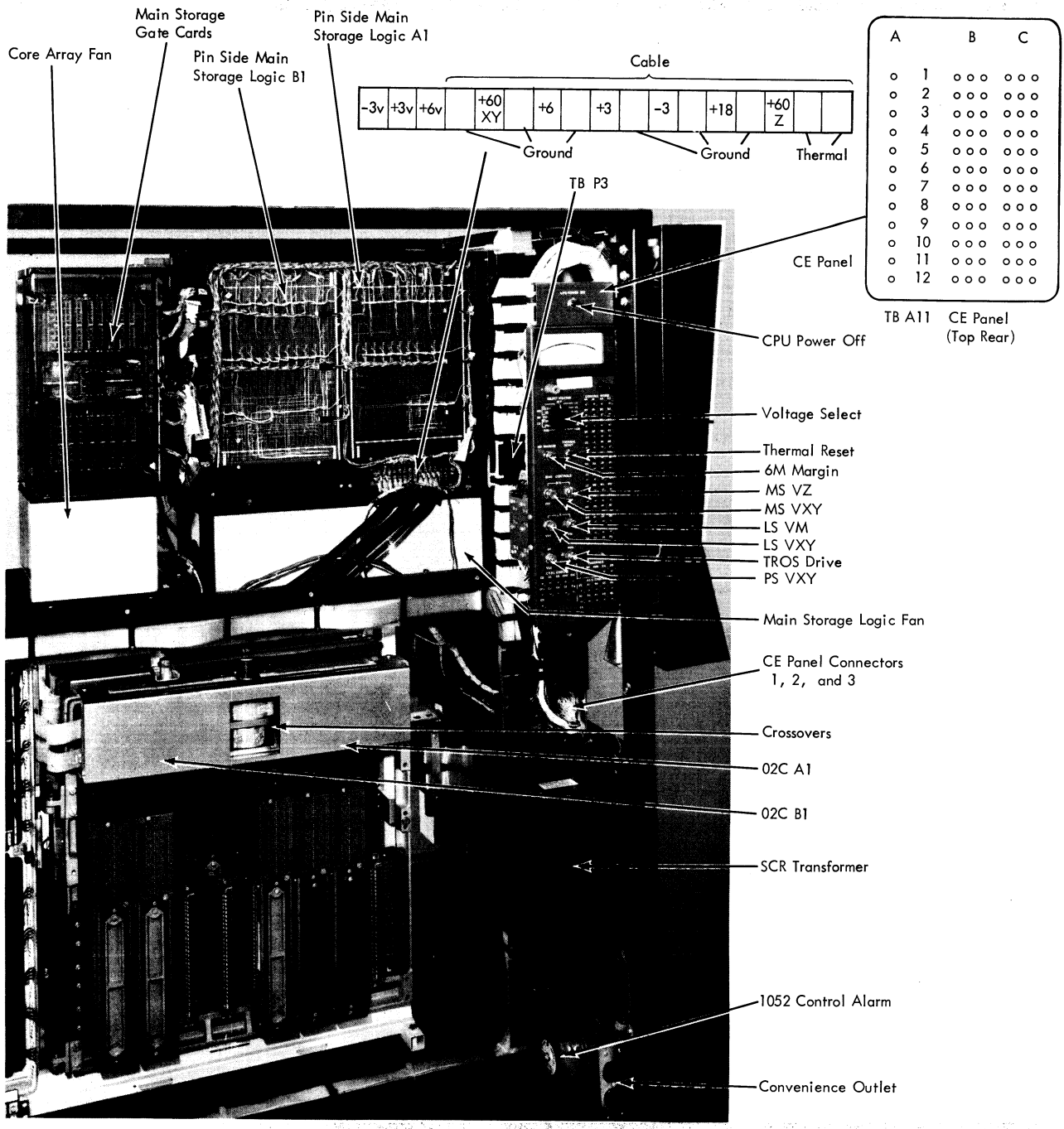


Figure 88. CPU — Left Side and Tailgate



	Ref Name	Location	ALD Sheet	
			High Frequency	Mid-Pac
Resets	Thermal	Internal CE Panel	PA 830	YC 158
	Overcurrent	CON/INV Unit (Power Supply)	YB 010	na
	Overvoltage	Power Supply Unit	YA080	na
Potientiometers	6M Margin	Internal CE Panel	PA 830	YC 158
	MS (VXY-VZ)	Internal CE Panel	PA 830	YC 158
	LS (VXY-VM)	Internal CE Panel	PA 830	YC 158
	PS (VXY)	Internal CE Panel	PA 830	YC 158
	TROS DRIVE	Internal CE Panel	PA 830	YC 158
	+48v	SMS Card 48v Module	YD 010	na
	Others			

Figure 89. CPU–Left Side

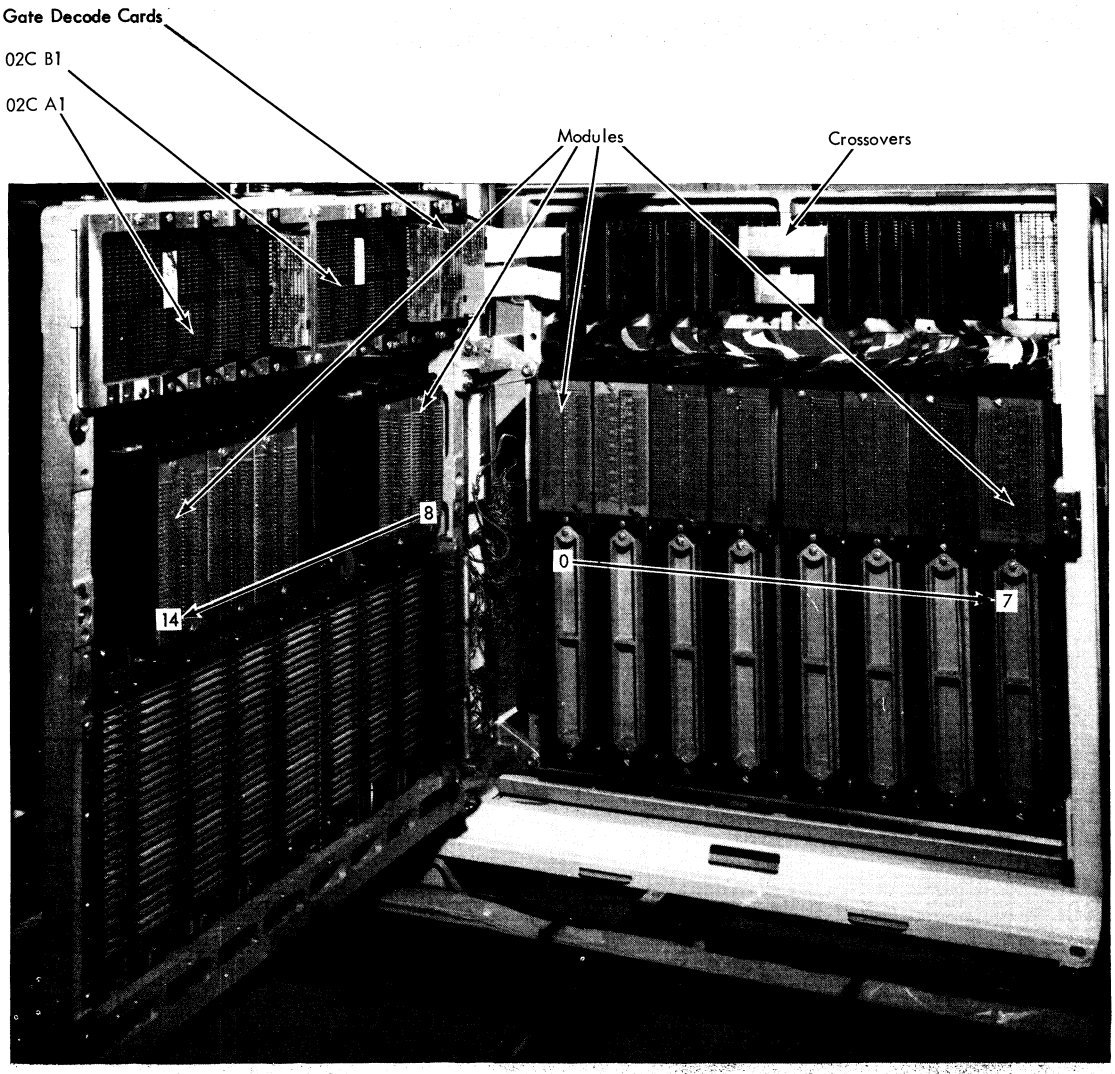


Figure 90. TROS Gates

Connectors

Tailgate Connectors (Figure 88)

All I/O connections to the CPU are made via the tailgate serpent connectors which are close to the CPU logic gate hinge.

This provides a suitable anchor point for the flexible tape cables to enter the tailgate. All connections to and from the tailgate are pluggable. Access to the CPU side of the tailgate is via the left side cover and to the I/O side by removing the cabinet end cover.

Mixer Panel Connections

All interconnections between the CPU and the console are made via the mixer panel which is at the console panel end of the CPU cabinet.

Tape connectors to the mixer panel are accessible via the left side. Pin connections are accessible by opening the CPU console panel.

IBM 1052 Connections

Connections to the CPU from the 1052 are made via the IBM 1052 interface connector. This is a serpent connector and is on the lower front end of the CPU. To the right of the IBM 1052 interface connector are the IBM 1052 power sockets, P and K.

Figure 87 shows the various connectors and their pin/socket numbering.

CE Panel Connectors

The internal CE panel connectors, 1, 2, and 3, are mounted on the inside of the front end of the CPU and are accessible from the left side doors (Figure 89).

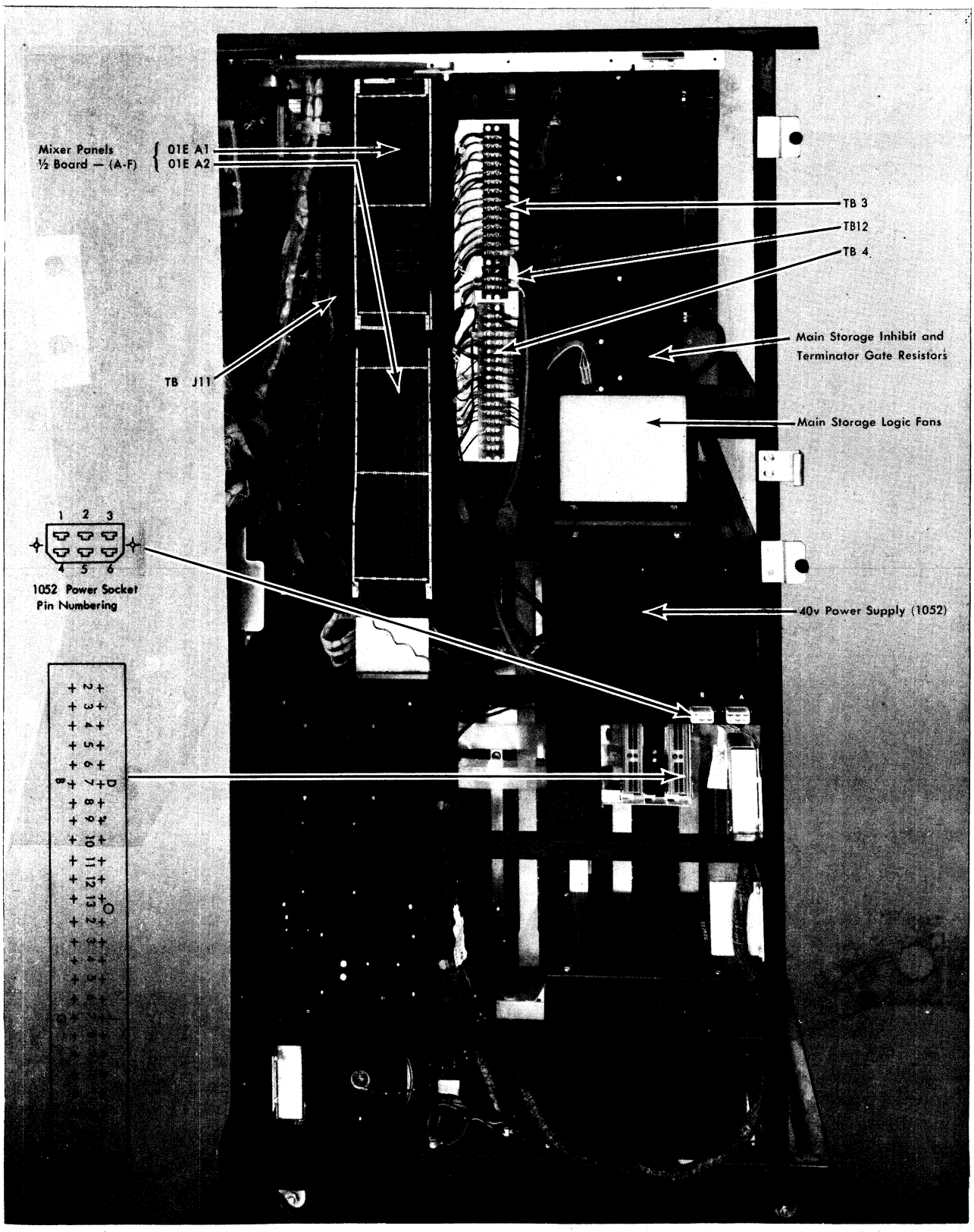


Figure 91. Console End (Doors Open)

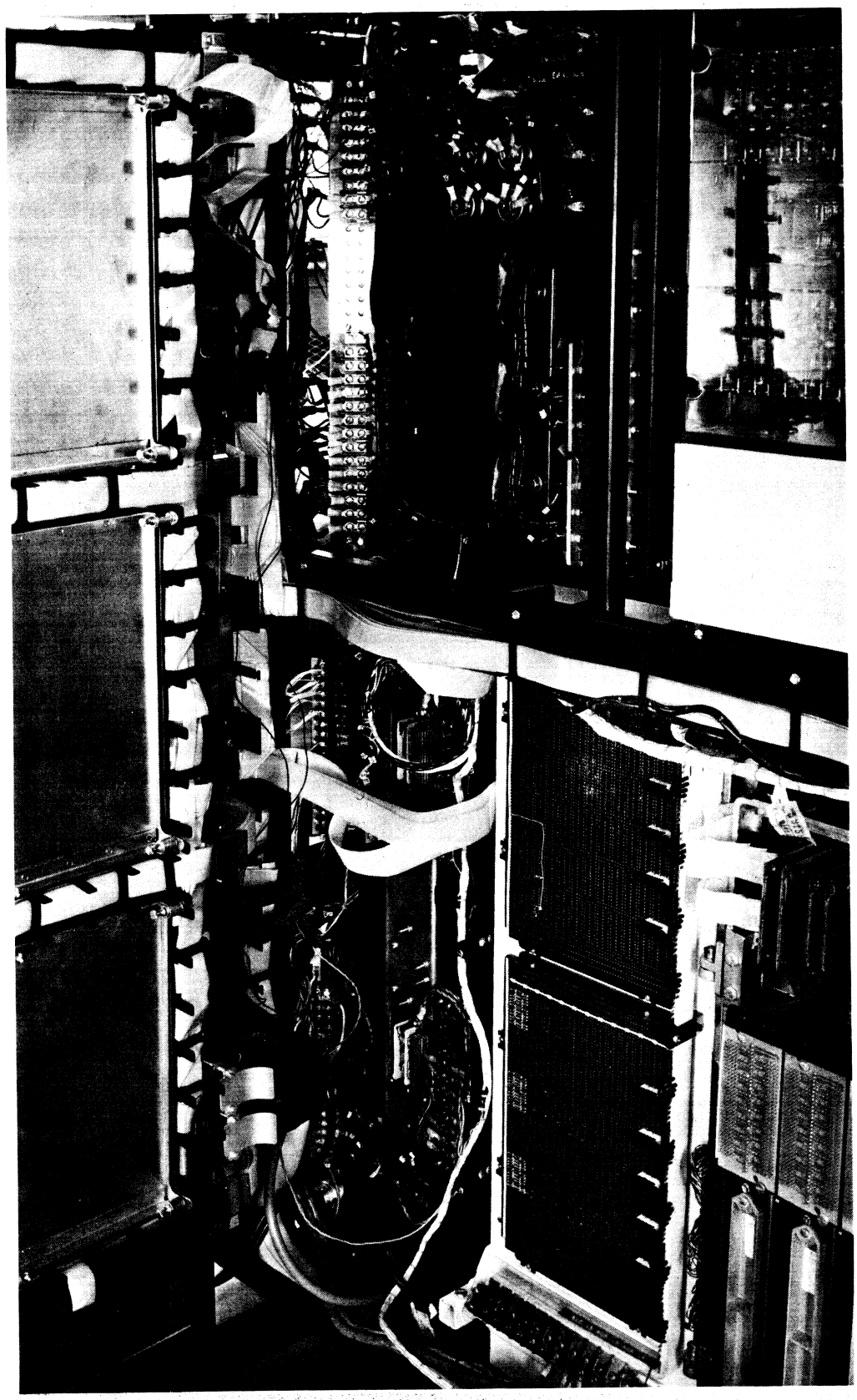


Figure 92. Mid-Pac Power Supply Unit, Sheet 1 (Rear)

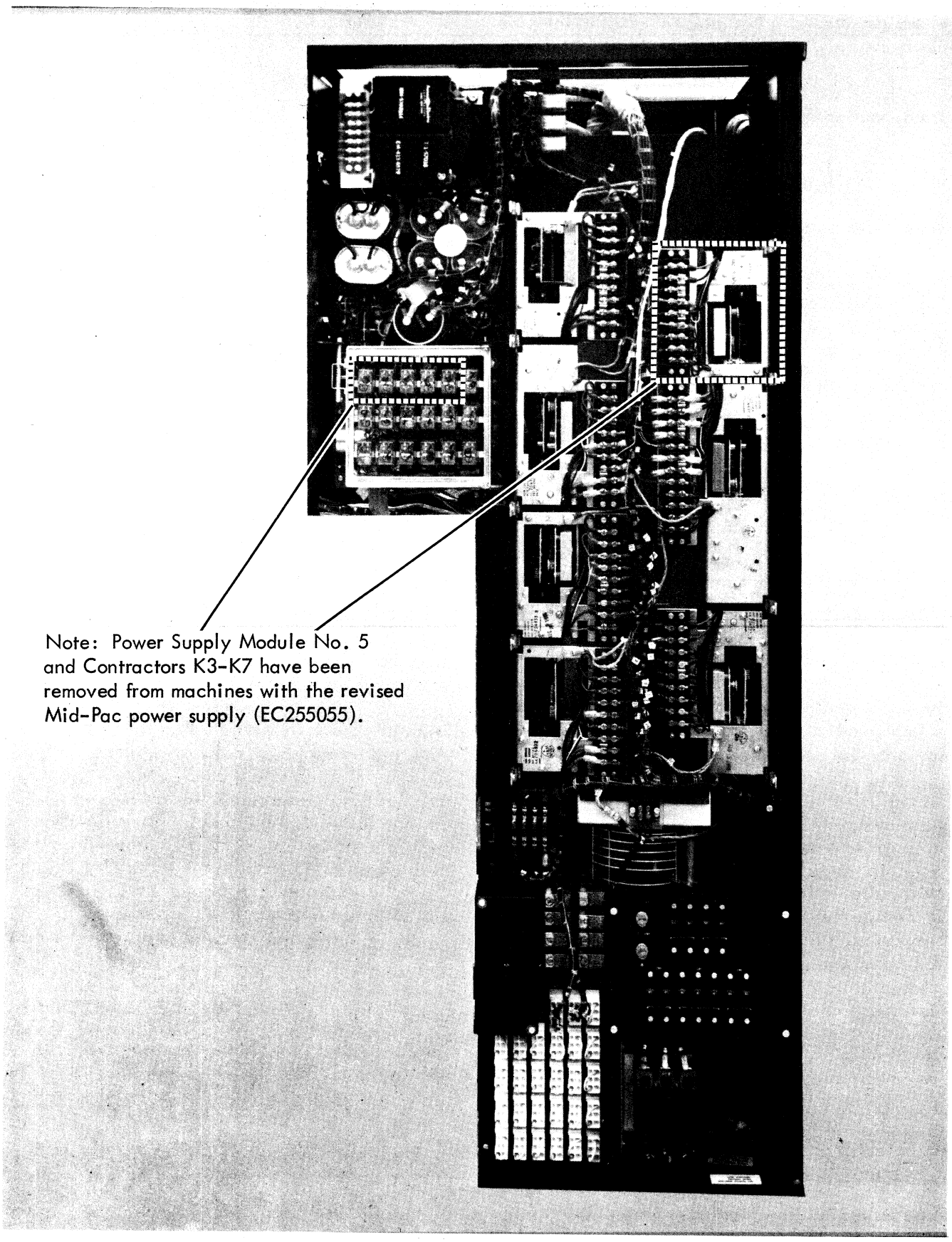
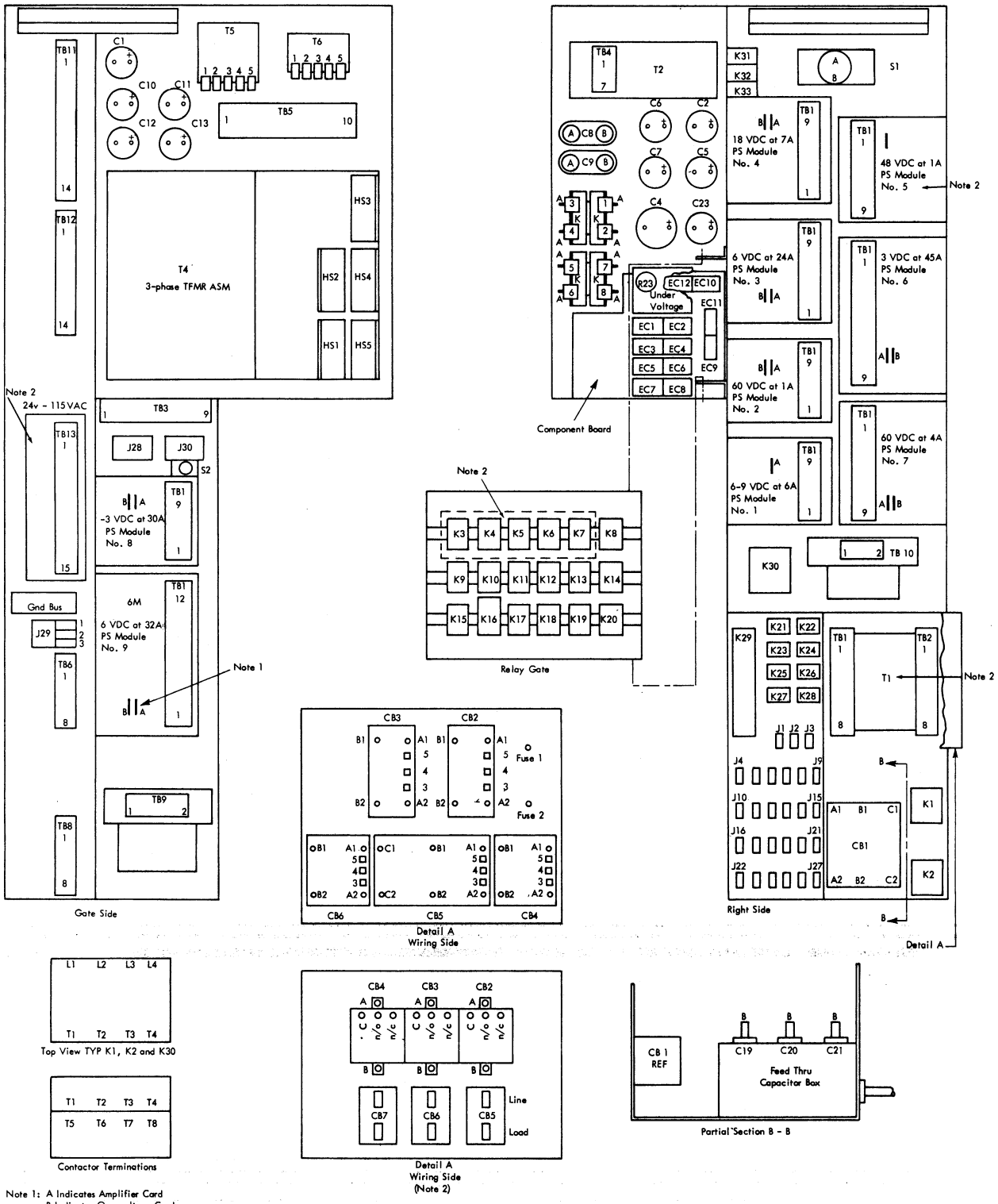


Figure 92. Mid-Pac Power Supply Unit, Sheet 2 (Right Side)



Note 1: A Indicates Amplifier Card
B Indicates Overvoltage Card

Note 2: Power supply No. 5, T1, and
Contactors K3-K7 have been removed
in the revised Mid-Pac power supply (EC255055).
A combined 24-115v supply has been added behind TB13.

Figure 93. Mid-Pac Power Supply Diagram

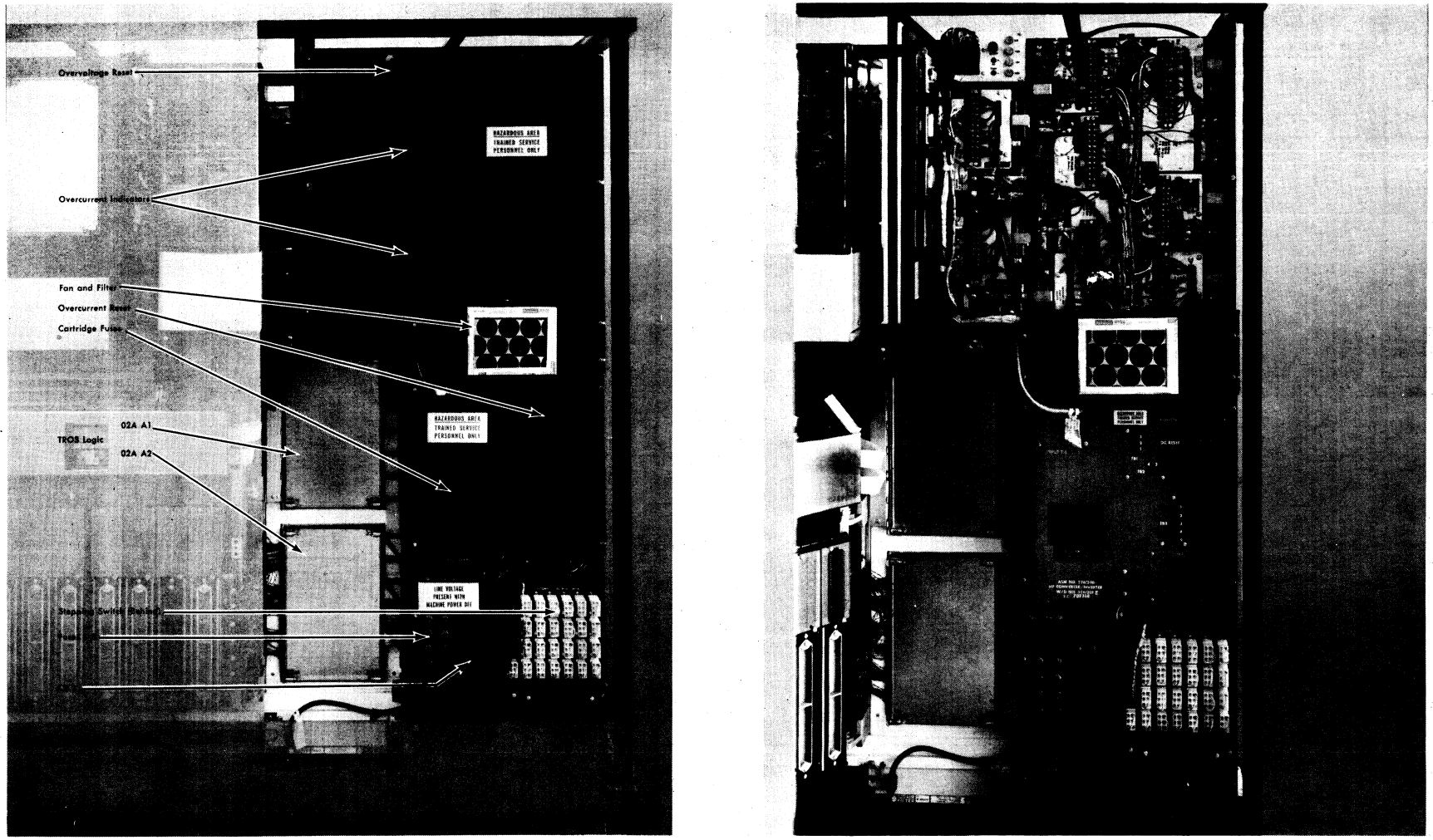


Figure 94. High Frequency Power Supply Unit

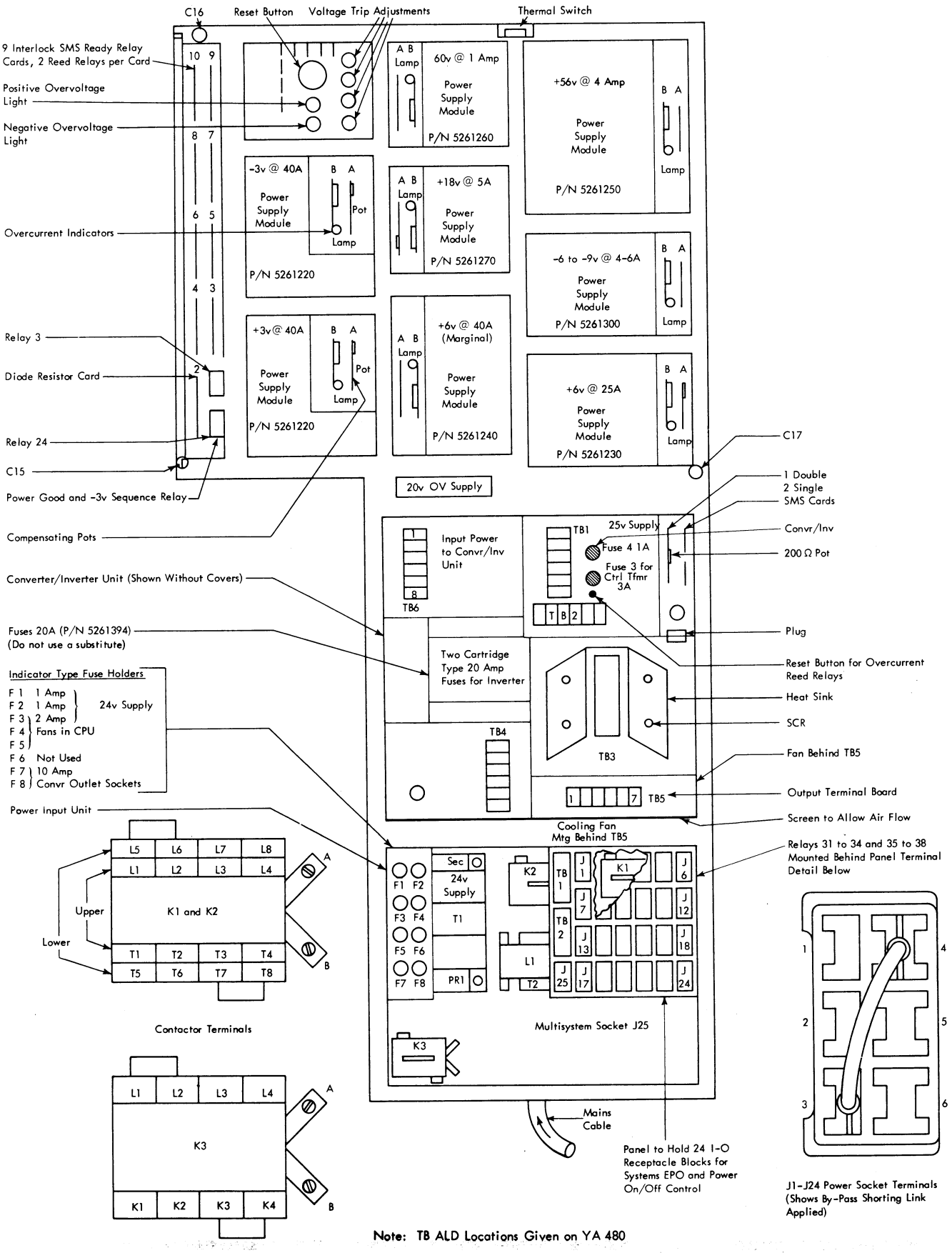
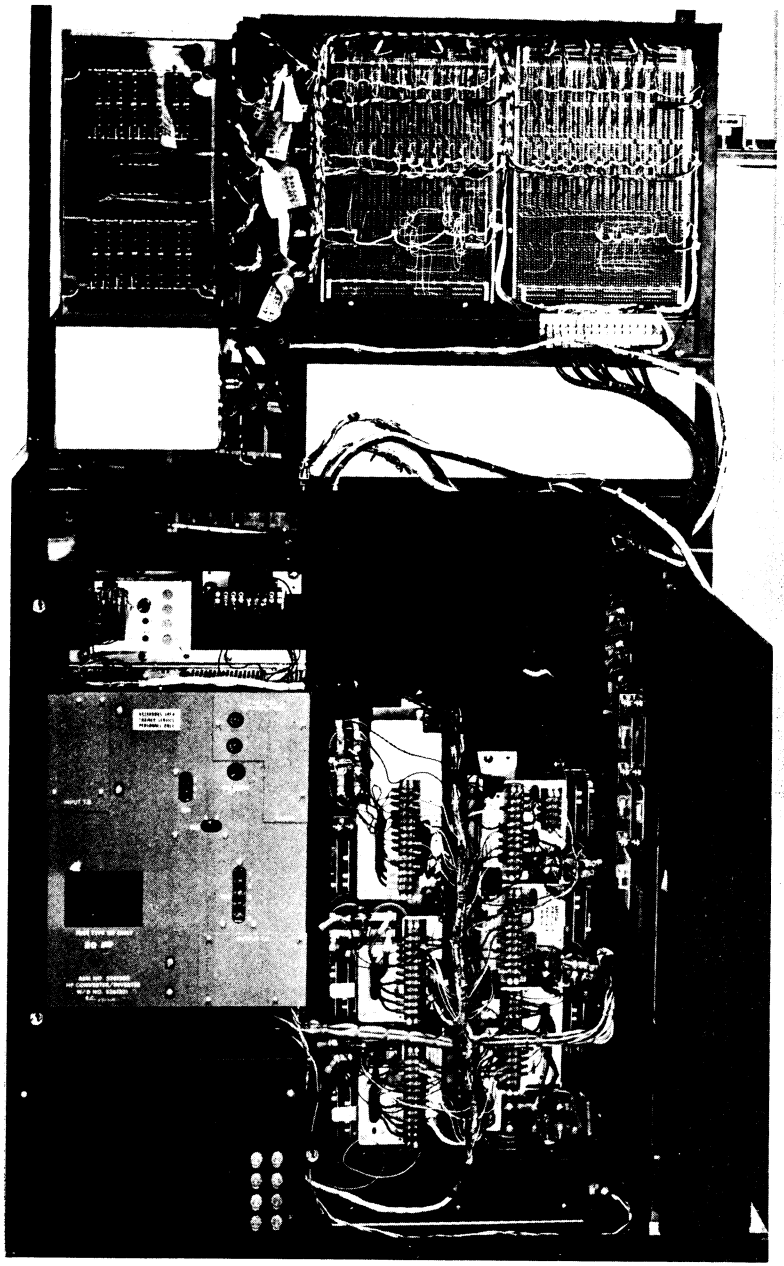
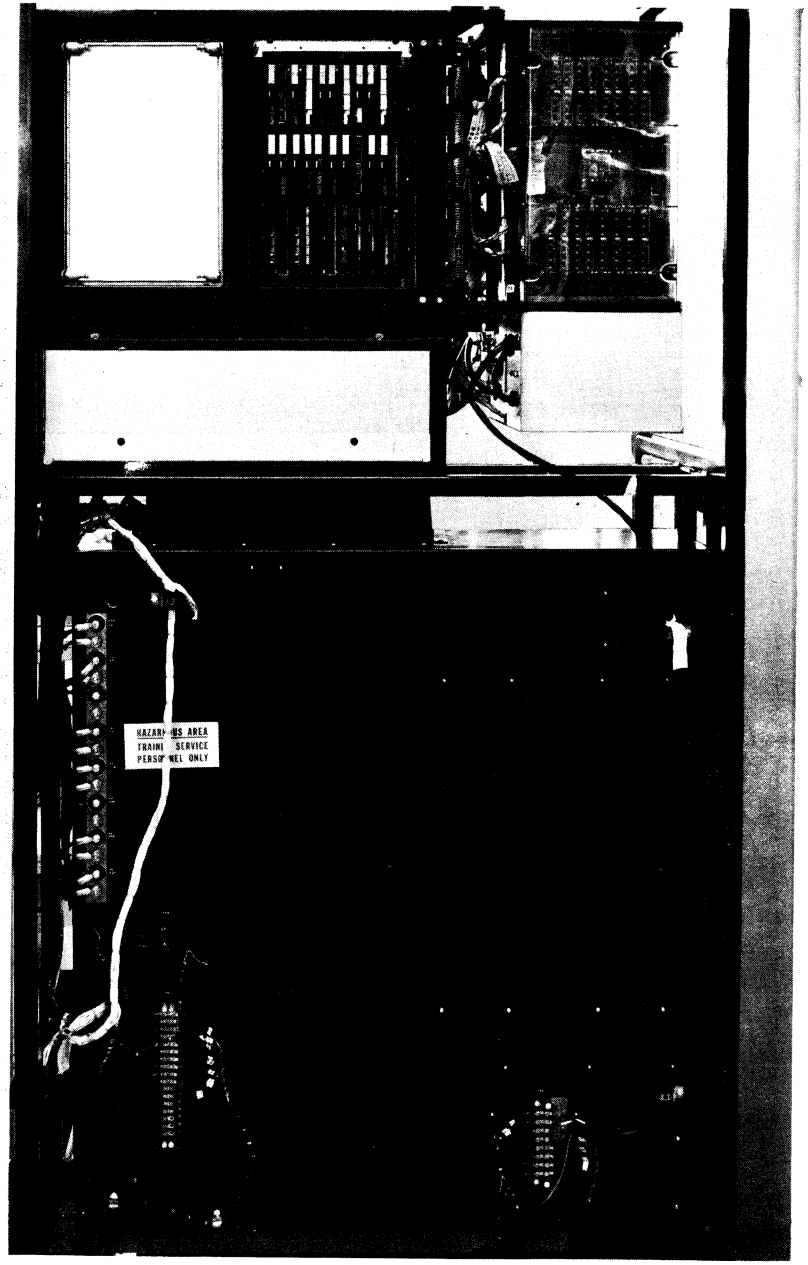


Figure 95. High Frequency Power Supply Diagram



Front



Rear

Figure 96. Wall Frame HF Power Supply

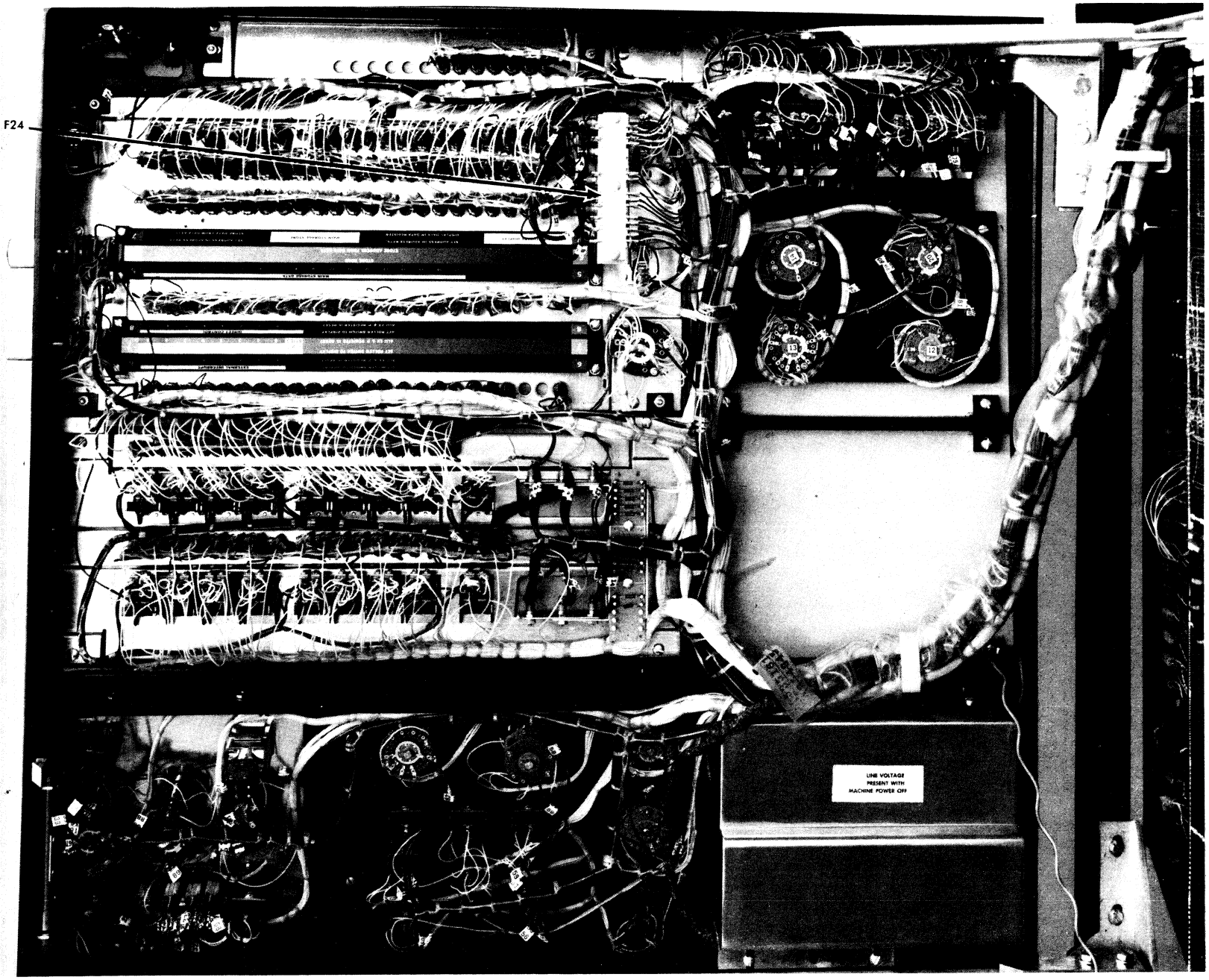


Figure 97. Console Panel (Rear View)

Console

System Control Panel

This section locates the various components which are found at the rear of the operator's console panel. See Figure 97.

CE Panel (Figure 89)

The CE panel is at the left side, console end of the CPU. Some connections to this panel from the CPU are made via sockets CE1, CE2 and CE3. See Figure 89.

NOTE: Behind the CE panel are:

Terminal blocks – A11, J11

Terminal posts – D11, W11

The TB A11 terminal block is shown in Figure 89.

TROS

The TROS logic and module arrays are mounted at the right side of the main frame and are accessible via the right side door. The TROS logic occupies two boards and is accessible via the hinged cover. The contact pins (rear of board) are accessible for scoping, etc., from the left side of the machine by swinging open the CPU logic gates. See Figures 87 and 90.

Module changes may be made easily, as both sides of the module array are accessible.

Main Storage

The main storage logic and core arrays are mounted at the right side of the main frame. Logic accessibility is similar to TROS, and core arrays may be swung open and accessed via the right-hand door for array 2 or by opening the CPU logic gates A and B for array 1. See Figures 87 and 89.

NOTE: The main storage logics contain physical location drawings.

Local Storage

1. Core plane arrays are in logic gate A.
2. Mounted on two, 4-72 SLT cards.
3. Located at 01A-D1.
4. Cards are *not* interchangeable.

Storage Protect

1. Core plane array is in logic gate A.
2. Mounted on a 4-72 SLT card.
3. Located at 01A-D1.

Boards and SLT Cards

The boards accommodate SLT cards, cross-over connectors, and cable connectors.

In the System/360 2040 Processing Unit, there are 12 such boards in CPU logic gate A and similarly in logic gate B.

Figure 98 shows boards labeled in gates. The addressing scheme of a board is shown in Figure 99. The location address scheme of SLT cards is shown in Figure 99.

Fuses

The power supplies are stacked in the rear right-hand corner of the CPU and a removable screen is fitted to prevent electrical radiation.

Figures 93 and 95 show the basic modular construction of the power supply. Figures 92 and 94 show the power supply layout within the main frame and the locations of the modules, SMS cards, fuses, and fan.

Fuse Chart HF (2.5 KC) Power Supply

FUSES	REFERENCE NAME	RATING	P/N	SYSTEM ALD
50-Cycle Supply	F1	1A	6325	YC 010
	F2	1A	6325	YC 010
	F3	6A	107667	YC 010
	F4	6A	107667	YC 010
	F5	6A	107667	YC 010
	CB2	10A	2092297	YC 010
	CB3	3.5A	889846	YC 010
	CB4	14A	8019397	YC 010
	CB5	7A	8021669	YC 010
60-Cycle Supply	F1	1A	6325	YB 010
	F2	1A	6325	YB 010
	F3	3A	6324	YB 010
	F4	3A	6324	YB 010
	F5	3A	6324	YB 010
	F6 Spare			
	F7	10A	511063	YB 010
	F8	10A	511063	YB 010
	CB1	20A	2130337	YB 010
Conv Inv	F3 (24v tfmr)	1A	P/N 303549	(Fig. 88)
	F4 (fan)	.25A	P/N 111261	(Fig. 88)
	F1 and F2	20A	P/N 5261394	(Fig. 88)

CAUTION

When replacing F1 and F2, be sure you use only the correct part number. *Do Not Substitute.*

Miscellaneous Components

Main Power Circuit Breaker (CB1)

The main power circuit breaker is near the bottom of the power supply unit. On a CPU with a 50-cycle power supply, this is a manually operated switch. The 60-cycle power supply contains a CB; the reset is visible and accessible without removing the covers. Refer to Figure 94.

Hinge — Gate A (Card Side)

	A	B	C	D
1	MPX Channel	Main Storage Controls, Clock, Checks	LSAR Log Out, *Storage Protect	Local Storage, *Storage Protect Local Stor
2	ROS	ROS	Data Flow	Data Flow
3	ROS Address Compare, and Stats	Interval Timer, ALU	ALU	Console Entries

Gate B (Card Side) — Hinge

	A	B	C	D
1		*Selector Channel 2	*1052	*1052
2	*Channel to Channel	*Selector Channel 2	*Selector Channel 1	*Selector Channel 1
3	*1401 or 1410 Translator *Direct Control	*Selector Channel 2	*Selector Channel 1	*Selector Channel 1

*Optional Feature

Figure 98. Board Layout of CPU Logic Gates

Indicators

The only indicators that are not on the main console or internal CE panel are those which indicate overcurrent or overvoltage.

The overcurrent indicators are one to each power supply module, on SMS cards adjacent to the respective power supply.

The overvoltage indicators L1 and L2 (positive and negative supplies respectively), are on the top left of the power supply unit. See Figures 94 and 95.

Potentiometers

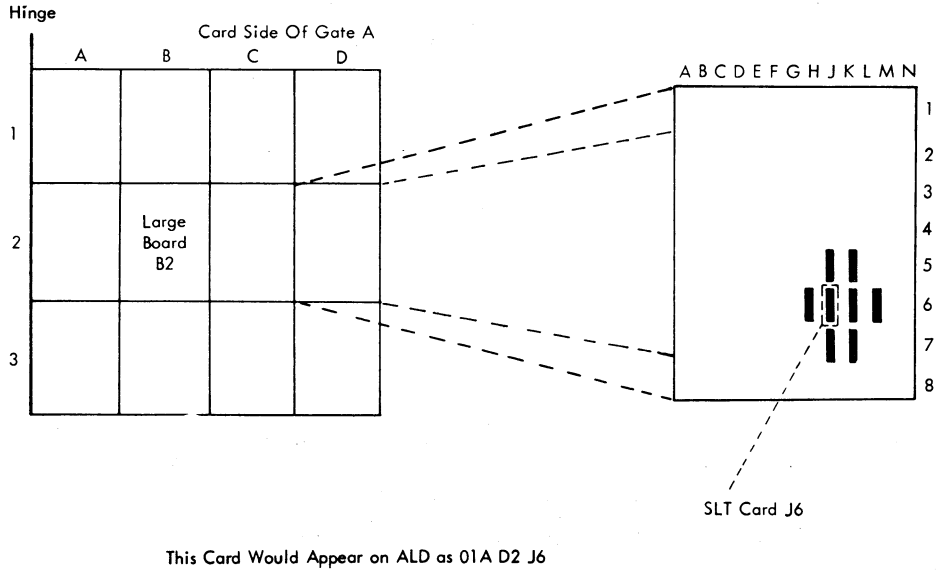
The DC voltage potentiometers in the power supply unit are on the SMS cards adjacent to the respective power supply modules. The overvoltage adjustment potentiometers are on the top left of the power supply unit. See Figures 94 and 95.

Laminar Bus

This is a bus connecting the power supply to the other main frame units.

The layout is:

1	2	3	4	5	6
Spare	Spare	Ground	+6v	Ground	−6v to −9v
7	**8**	**9**	**10**	**11**	**12**
Ground	+6v Margin	Ground	−3v	Ground	+3v



This Card Would Appear on ALD as 01A D2 J6

Figure 99. SLT Card and Board Addressing Scheme

The laminar bus is terminated by terminal blocks which have the same connection layout. Terminal blocks within the power supply unit have similar numbers and, therefore, must be referenced to a particular module or unit. For example, TB4 C1 Unit.

Terminal blocks outside the power supply unit are shown in "Locations." Locations of voltages on buses and terminal blocks, within main frame units, are not necessarily the same as the main laminar bus. They should be checked before use.

Relay and SMS Card Sockets

Figures 93 and 95 show the socket pin allocation for the medium sized relays and the power supply SMS cards.

Manual Resets

The power supply manual resets are:

REFERENCE NAME	LOCATION	SYSTEM ALD
Thermal	CE Panel	PA 830
Overcurrent	Power Supply	None
Overvoltage	Power Supply	YA 311

Special Feature Additive Card Codes

Additional SLT cards are wired for some special features. The second line of ALD blocks contains the additive card codes for these special features (Figure 100).

Version Number	Feature	Additive Card Code
000	Basic	
001	Table Address Chaining (TAC)	TAC
002	Floating-Point Arithmetic	FPA
003	Decimal Arithmetic	DEC
005	SUMP with Translate Halfword	
007	B200 Simulator Assist	
010	Non-IBM Meter	
011	Simulator 705 Assist	
012	Mpx Channel Extension	
013	256 UCW's	
014	Move Inverse Instruction (WTC)	
017	301 Simulator Assist	
020	Interval Timer 50 Hz	TIM
022	Interval Timer 60 Hz	TIM
023	1.2-Microsecond Timer	
025	Measurement Interface	
026	13-Microsecond Timer	
031	1401/1440/1460 DOS Compatibility	
033	Interruption Power Failure	
035	Direct Control External Interrupt	
036	GE 225 Simulator	
043	Selector Channel 1	SC1B
050	Storage Protect	SP
050	Storage Protect SC1	STC 0
050	Storage Protect SC2	STC 1
051	Storage Protect on Read	
053	1410 Emulator 100K	
060	Direct Control	DCT
065	*UNIVAC Simulator	
066	Test Zero Condition	
069	**Program Trace**	
071	16K Storage (Model D)	ST 1
072	32K Storage (Model E)	ST 2
073	64K Storage (Model F)	ST 3
074	128K Storage (Model G)	ST 4
075	256K Storage (Model H)	ST 5
076	Storage Size Switch	
079	**192 UCW's**	
080	External Interrupt	
087	Instruction Terminate Move by Character	
088	Enable ROS Control Data	
089	LASA Data Set	
091	1401 Emulator	CLC
092	1410 Emulator	CBS4
093	Sum of Products (SUMP)	
097	Associative Memory (Cambridge Time-Sharing)	
098	1401/1311 Emulator	
099	Extended I-Fetch	
107	Expanded Addressing Capability	
A01	Versions 001 and 093	
A13	Versions 013 and 092	
A23	Versions 025 and 092	
A26	Versions 025 and 026	
A31	Versions 031 and 092	
A33	Versions 033 and 051	SC2B
A44	SC2	
A52	Halfword Translate with Version 043	
A53	Versions 101 and 092	
A79	Versions 079 and 092	
A97	Cambridge Time-Sharing (TROS Version)	
F91	Emulator Module 7 (TROS Version)	
J40	1410 Emulator (40K)	
L89	Versions 002 and 089	
M33	Versions 033 and 051	
M66	Versions 043 and 066	
R01	Versions 001 and 043 (TROS Version)	
R11	Versions 002, 005, and 099	
R15	Versions 092, 043, and 014 (WTC)	
P15	Versions 014, 015, 002, 050, 091, and 098 (WTC)	

1052 Versions

000	Non-SIPO	
001	SIPO	
	Time-Out (Model 65 and Larger Systems)	LRG
	2150 Metering Console Adapter	MTR

*Trademark of Sperry Rand Corporation

Figure 100. Version Numbers and Additive Card Codes

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